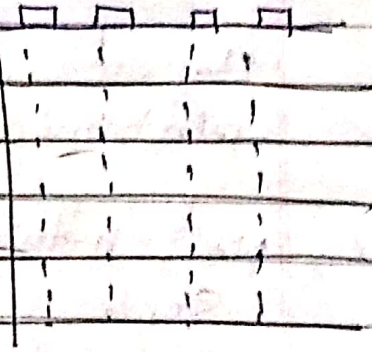
Section-1

Que 2.

Ans:- The truth table for the function then the JK flip-flop is Basically an SR flip-flop with feed back which enables only one of its two input terminals, either set or Reset to be active at any one time there by eliminating the invalid Condition. Seen previously in the SR flip flop circuits.

Present State	Next State		output(z)		Mode
	x=0	x=1	x=0	x=1	
000	100	101	0	0	θ_1
001	100	101	0	1	θ_1
010	000	000	1	0	θ_2
011	000	000	0	1	θ_2
100	111	110	1	0	2
101	110	110	0	1	
110	011	010	1	0	
111	011	011	0	1	



$Q_1\ Q_2\ Q_3 = 00$

Flip flops → rising edge triggered

input change midway between edge of the clk

What is 3 bit up down counter

Synchronous 2-bit / down counter.

This is achieved by using and additional input pin which determines the direction of the count,

either up or down and the the timing diagram gives an example of the counter operation of this up/down input changing state.

Why JK flip-flop of flip flop

T-flip - flop is also - To make flip flop to avoid the occurrence of intermediate state. in SR flip-flop.

we should provide only one inp the flip-flop called.