SEC-2

① Enlist and explain the interrupt pins in 8085. Explain the addressing modes of 8085.

Interrupt pins in 8085 :-
Hardware interrupts :-

i) TRAP :-
a) It is non-maskable interrupt. In order to service this interrupt the signal on TRAP pin must have high level.
b) If this condition occur then 8085 completes execution of current instruction, pushes the program counter on the stack and branches to location 0024H

ii) RST 7.5 :-
a) It is maskable interrupt. It can be enabled and disabled using SIM instruction.
b) In order to service RST 7.5 8085 complete current execution of instruction, pushes the program counter on to the stack and branches to 003CH.

iii) RST 6.5 :-
a) This can be enabled and disabled using SIM instruction.
b) RST 6.5 is high level sensetive, microprocessor 8085 execute current instruction, save the program counter on to the stack and branches to location 0034H.

iv) RST 5.5 :-
a) It is maskable interrupt and can enabled and disabled by SIM instruction. It is high level sensetive.
b) In order to service this interrupt 8085 completes the execution of current instruction, save the program counter on to the stack and branches to location 002CH.

v) INTR :-

a) It is non-maskable interrupt. whenever INTR Signal, external logic places completes its current instruction and send activate low interrupt acknowledge Signal INTA

Software Interrupt :-

Interrupt type	Hex code	vector address
RST 0	C7	0000H
RST 1	CF	0008H
RST 2	D7	0010H
RST 3	DF	0018H
RST 4	E7	0020H
RST 5	EF	0028H
RST 6	F7	0030H
RST 7	FF	0038H

Addressing modes of 8085 :-

1) Immediate addressing mode :-
In immidiate addressing mode the operand is specified within the instruction itself.

b) importance :- In the immidiate addressing mode, the data is stored along with the instruction and the data is directly transfer to the register.

c) Example :- MVI A, 05H

2) Register addressing mode :-
a) The register addressing mode specifies the source operand destination operand or both to be contained in an 8085 registers.

b) importance :- In this mode the data is copied from one register and stored in another register.

c) Example :- MOV A, B

3) Direct addressing mode :-
a) The direct addressing mode specifies the 16-bit address of operand within the instruction itself.

b) Example :- LDA 2000H

(4) Indirect addressing mode :-

a) Indirect addressing mode. the memory address where the operand located is specified by the contents of a register pair.

b) Example :- LDAX B

(5) Implied or Implict addressing mode :-

a) In Implied addressing mode. opcode specifies the address of the operands

b) Example :- CMA