Roll No. | | | | | | | | | | |

SHAMBHUNATH INSTITUTE OF ENGINEERING AND TECHNOLOGY

Subject : Digital System Design Subject Code : KEC302

B.Tech. 3rd SEMESTER

FIRST SESSIONAL EXAMINATION, ODD SEMESTER, (2019-2020)

Branch : Electronics & Communication Engineering

Time –1hr 30 min **Maximum Marks – 30**

SECTION - A

Q-1) Attempt ALL parts- **(5*1 = 05)**

a) Perform the following conversions : (A) $(101000100111)_2 = (\ ?\ )_{10}$ (B) $(511)_{10} = (\ ?\ )_8$

b) State De Morgan's theorem.

c) How many 3:8 line decoder with enable input are required to construct 6:64 line decoder without using any other logic?

d) Explain magnitude comparator?

e) Differentiate between combinational and sequential circuits.

SECTION - B

Q 2) Attempt any TWO parts from this section. **(2*5 = 10)**

a. Determine the POS expression using K-map.

$$f = x'z' + wyz + w'y'z' + x'y$$

b. Implement a full subtractor using two 4:1 Multiplexer.

c. Design a 4 bit parallel adder circuit by using full adder.

d. Explain the operation of a SR flip-flop.

SECTION - C

3. Attempt any ONE part of the following : **(1*5 = 5)**

a) Minimized the expression and Realize the expression using NAND gate only.
F(A,B,C,D,E) = ∑m (1, 3, 4, 5, 11, 12, 14, 16, 20, 21, 30)

b) Minimize the following function using Quine-McClusky method:

F (A,B,C,D)=∑m(0,3,5,6,7,10,12,13) + d (2,9,15)

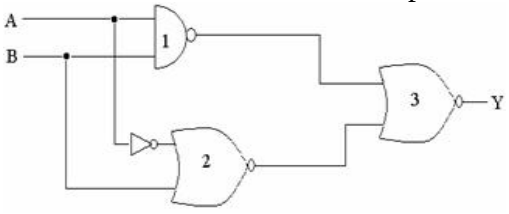
4. Attempt any ONE part of the following : **(1*5 = 5)**

a) Implement the following function using a 3 to 8 line decoder $F_1 = \sum(3,5,6,7)$ and $F_2 = \sum(1,2,4,7)$

b) Using 8:1 MUX with A as input line, realize the following function with multiplexer.
F(A,B,C,D) = ∑m (0,1,2,4,6,9,12,14)

5. Attempt any ONE part of the following : **(1*5 = 5)**

a) Analyze the logic circuit shown below and determine the output Y.



b) Design an 8-bit adder/subtractor using ALU 74181s in cascade. Show how it works if A=97 and B=29.

Solution Subject : Digital System Design Subject Code : KEC302

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SECTION - A

Q-1) ANSWERS **(5*1 = 05)**

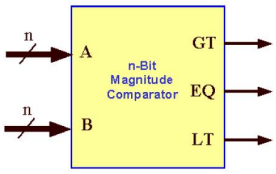
a) **ANS :** conversions : (A) $(101000100111)_2$ = (**2599**)$_{10}$ (B) $(511)_{10}$ = (**777**)$_8$

b) **ANS :** The complement of the product of two or more variables is equal to the sum of the complements of the variables.

$$\overline{A+B} = \overline{A}\cdot\overline{B} \quad \text{OR} \quad \overline{A\cdot B} = \overline{A}+\overline{B}$$

c) **ANS : NINE** 3:8 line decoder with enable input are required to construct 6:64 line decoder without using any other logic.

d) **ANS :** A magnitude comparator is a combinational circuit that compares two numbers A & B to determine whether: A > B, or A = B, or A < B



e) ANS :

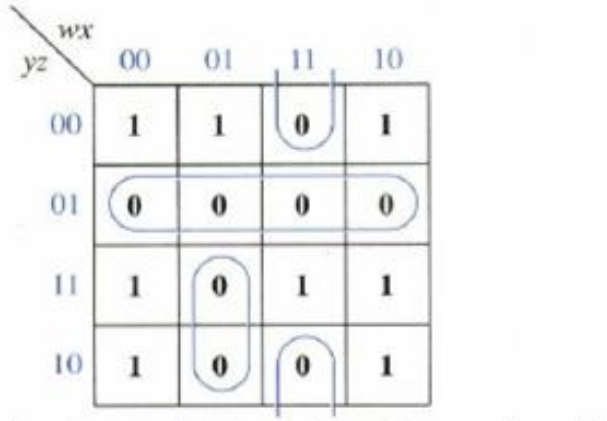
A combinational system (device) is a digital system in which the value of the output at any instant depends only on the value of the input at that same instant (and not on previous values).

A sequential circuit is a circuit with memory. A sequential circuit is said to be synchronous if the internal state of the machine changes at specific instants of of time as governed by a clock.

SECTION - B

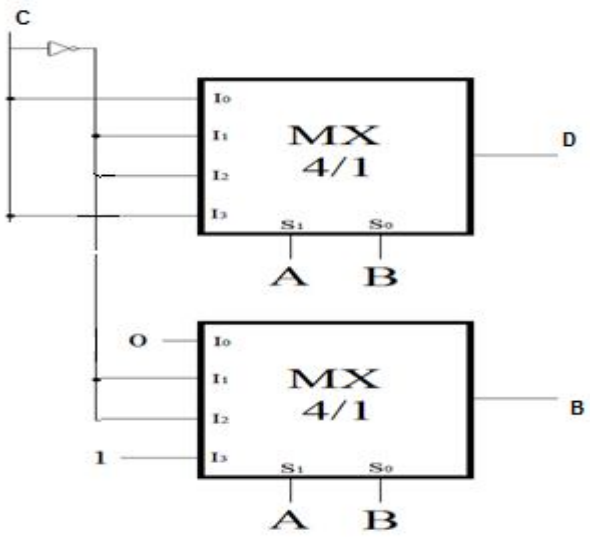
Q 2) Attempt any TWO parts from this section. **(2*5 = 10)**

a. ANS : The POS expression using K-map.



$$f = (y + z')(w' + x' + z)(w + x' + y')$$

b. ANS : Full subtractor using two 4:1 Multiplexer.

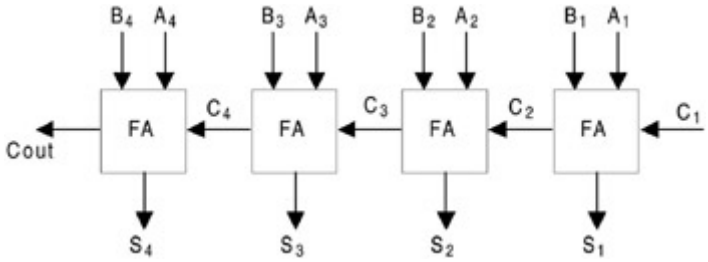


Truth Table

C	B	A	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

c. ANS : A 4 bit parallel adder circuit by using full adder.

d.



e. ANS : operation of a SR flip-flop.

From the diagram it is evident that the flip flop has mainly four states. They are

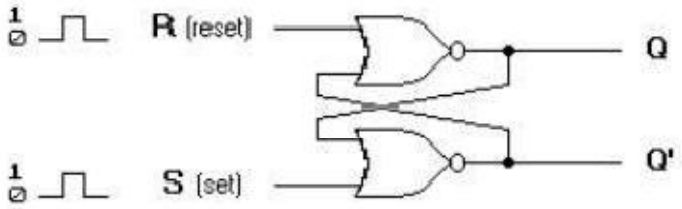
S=1, R=0—Q=1, Q'=0 This state is also called the SET state.

S=0, R=1—Q=0, Q'=1 This state is known as the RESET state.

S=0, R=0—Q & Q' = previous state.

S=1, R=1—Q=0, Q'=0 [Invalid]

This is an invalid state because the values of both Q and Q' are 0. They are supposed to be compliments of each other. Normally, this state must be avoided.



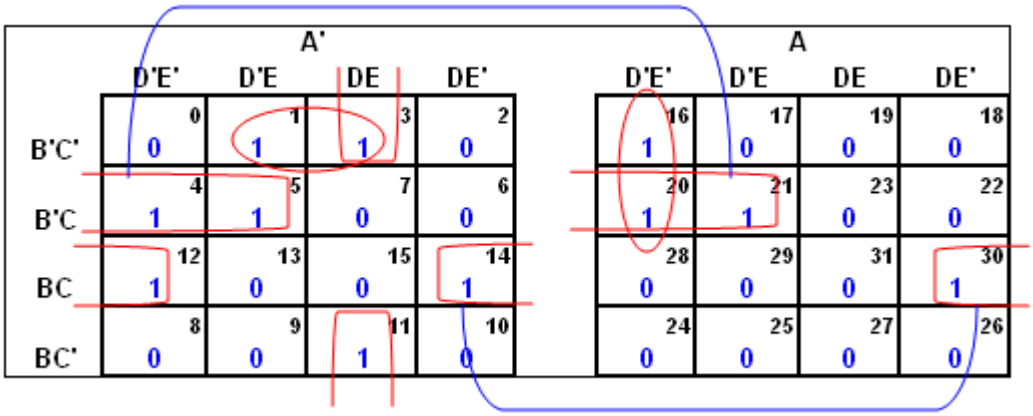
(a) Logic diagram

S R	Q Q'	
1 0	1 0	
0 0	1 0	(after S=1, R=0)
0 1	0 1	
0 0	0 1	(after S=0, R=1)
1 1	0 0	

SECTION - C

3. Attempt any ONE part of the following : **(1*5 = 5)**

a) F = B'CD' + A'BCE' + BCDE' + A'C'DE + AB'D'E' + A'B'C'E



b) **ANS :** Quine-McClusky method:

For Minterms:

Minterm ID	W	X	Y	Z
0	0	0	0	0
3	0	0	1	1
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
10	1	0	1	0
12	1	1	0	0
13	1	1	0	1

For don't cares:

Minterm ID	W	X	Y	Z
2	0	0	1	0
9	1	0	0	1
15	1	1	1	1

Groups	Minterm ID	W	X	Y	Z	Merge Mark
G0	0	0	0	0	0	
G1	2	0	0	1	0	
G2	3	0	0	1	1	
	5	0	1	0	1	
	6	0	1	1	0	
	9	1	0	0	1	
	10	1	0	1	0	
	12	1	1	0	0	
G3	7	0	1	1	1	
	13	1	1	0	1	
G4	15	1	1	1	1	

Groups	Minterm ID	W	X	Y	Z
G0'	0, 2	0	0	d	0
G1'	2, 3	0	0	1	d
	2, 6	0	d	1	0
	2, 10	d	0	1	0
G2'	3, 7	0	d	1	1
	5, 7	0	1	d	1
	6, 7	0	1	1	d
	5, 13	d	1	0	1
	9, 13	1	d	0	1
	12, 13	1	1	0	d
G3'	7, 15	d	1	1	1
	13, 15	1	1	d	1

Groups	Minterm ID	W	X	Y	Z	Merge Mark
G0'	0, 2	0	0	d	0	
G1'	2, 3	0	0	1	d	✓
	2, 6	0	d	1	0	✓
	2, 10	d	0	1	0	
G2'	3, 7	0	d	1	1	✓
	5, 7	0	1	d	1	✓
	6, 7	0	1	1	d	✓
	5, 13	d	1	0	1	✓
	9, 13	1	d	0	1	
	12, 13	1	1	0	d	
G3'	7, 15	d	1	1	1	✓
	13, 15	1	1	d	1	✓

Groups	Minterm ID	W	X	Y	Z
G1"	2, 3, 6, 7	0	d	1	d
	2, 6, 3, 7	0	d	1	d
G2"	5, 7, 13, 15	d	1	d	1
	5, 7, 13, 15	d	1	d	1

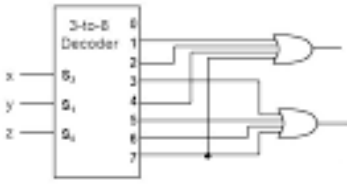
Groups	Minterm ID	W	X	Y	Z	Merge Mark
G0"	0, 2	0	0	d	0	
G1"	2, 3, 6, 7	0	d	1	d	
	2, 10	d	0	1	0	
G2"	5, 7, 13, 15	d	1	d	1	
	9, 13	1	d	0	1	
	12, 13	1	1	0	d	

Minterm ID	$\overline{W}\,\overline{X}\,\overline{Z}$	$\overline{W}Y$	$\overline{X}Y\overline{Z}$	XZ	$WX\overline{Y}$	$W\overline{Y}Z$
0	1					
3		1				
5				1		
6		1				
7		1		1		
10			1			
12					1	
13				1	1	1

$$F(W,X,Y,Z) = \overline{W}\,\overline{X}\,\overline{Z} + \overline{W}Y + \overline{X}Y\overline{Z} + XZ + WX\overline{Y}$$

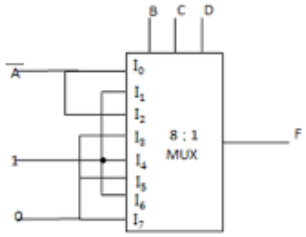
4. Attempt any ONE part of the following : (1*5 = 5)

c) Implement the function using a 3 to 8 line decoder. $F_1(x,y,z) = \sum(3,5,6,7)$ and $F_2(x,y,z) = \sum(1,2,4,7)$



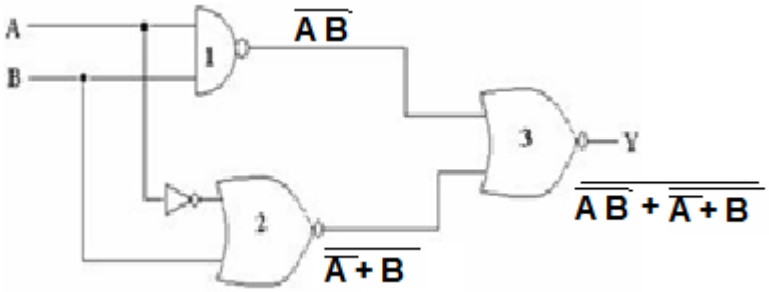
d) Using 8:1 MUX with A as input line, realize the following function with multiplexer.
$F(A,B,C,D) = \sum m(0,1,2,4,6,9,12,14)$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	$\bar{A}$	1	$\bar{A}$	0	1	0	1	0



5. Attempt any ONE part of the following : (1*5 = 5)

a) Analyze the logic circuit shown below and determine the output Y.



b) **Solution :** For designing an 8-bit adder/subtractor, two 74181 ICs are to be cascaded.

- The least-significant four bits of A & B are applied at the A & B inputs of the LSB 74181 and the most-significant four bits of A & B are applied at the A & B inputs of the MSB 74181.
- The carry-out of the least-significant 74181 is connected to the carry-in of the most-significant 74181.
- The 8-bit output will be available on F outputs.
- The select lines of both the 74181s are connected together.
- Addition if performed with M=0 and S=1011, and
- subtraction is performed with M=0 and S = 0110.
- Connect C_n of least-significant 74181 to 1 for addition and 0 for subtraction.

(a) A=97 = 01100001 B=29 = 00011101

Mode control M	Select inputs $S_3S_2S_1S_0$	least-significant ALU					Most-significant ALU					Output	Remark
		Inputs			Outputs		Inputs			Outputs			
		A_L	B_L	C_{in}	S_L	C_{n+4}	A_H	B_H	C_{in}	S_H	C_{n+4}		
0	1001	0001	1101	1	1110	1	0110	0001	1	0111	1	01111110	$(126)_{10}$
0	0110	0001	1101	0	0100	1	0110	0001	1	0100	0	01000100	$(68)_{10}$