NOTES

SUBJECT: INTRODUCTION TO MICROPROCESSORS

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INDEX

CHAPTER 1

UNIT 1

1.1 INTRODUCTION TO MICROPROCESSOR: Microprocessors are regarded as one of the most important devices in our everyday machines called computers. Before we start, we need to understand what exactly microprocessors are and their appropriate implementations. Microprocessor is an electronic circuit that functions as the central processing unit (CPU) of a computer, providing computational control. Microprocessors are also used in other advanced electronic systems, such as computer printers, automobiles, and jet airliners Typical microprocessors incorporate arithmetic and logic functional units as well as the associated control logic, instruction processing circuitry, and a portion of the memory hierarchy. Portions of the interface logic for the input/output (I/O) and memory subsystems may also be infused, allowing cheaper overall systems. While many microprocessors and single-chip designs, some high-performance designs rely on a few chips to provide multiple functional units and relatively large caches. When combined with other integrated circuits that provide storage for data and programs, often on a single semiconductor base to form a chip, the microprocessor becomes the heart of a small computer, or microcomputer. Microprocessors are classified by the semiconductor technology of their design (TTL, transistor-transistor logic; CMOS, complementary-metal-oxide semiconductor; or ECL, emitter-coupled logic), by the width of the data format (4-bit, 8-bit, 16-bit, 32-bit, or 64-bit) they process; and by their instruction set (CISC, complex-instruction-set computer, or RISC, reduced-instruction-set computer; see RISC processor). TTL technology is most commonly used, while CMOS is preferred for portable computers and other battery-powered devices because of its low power consumption. ECL is used where the need for its greater speed offsets the fact that it consumes the most power. Four-bit devices, while inexpensive, are good only for simple control applications; in general, the wider the data format, the faster and more expensive the device. CISC processors, which have 70 to several hundred instructions, are easier to program than RISC processors, but are slower and more expensive.

Microprocessors have been described in many different ways. They have been compared with the brain and the heart of humans. Their operation has been likened to a switched board, and to the nervous system in an animal. They have often been called microcomputers. The original purpose of the microprocessor was to control memory. That is what they were originally designed to do, and that is what they do today. Specifically, a microprocessor is “a component that implements memory.

A microprocessor can do any information-processing task that can be expressed, precisely, as a plan. It is totally uncommitted as to what its plan will be. It is a truly general-purpose information-processing device. The plan, which it is to execute—which will, in other words, control its operation —is stored electronically. This is the principle of “stored program control”. Without a program the microprocessor can do nothing. With one, it can do anything. Furthermore, microprocessors can only perform information-processing tasks. To take action on the outside world, or to receive signals from it, a connection must be provided between the microprocessor’s representation of information (as

digital electronic signals) and the real world representation.

4-BIT MICROPROCESSORS:

Historically, the 4-bit microprocessor was the first general-purpose microprocessor introduced on the market. The basic design of the early microprocessors was derived from that of the desk calculator. The Intel 4004, a 4-bit design, was the grandfather of microprocessors. Introduced in

late 1971, the 4004 was originally designed for a Japanese manufacturer as the processing element of a desk calculator; it was not designed as a general-purpose computer. The shortcomings of the 4004 were recognized as soon as it was introduced. But it was the first general-purpose computing device on a chip to be placed on the market. Many of the chips introduced at about the same time by other companies were, in fact, mere calculator chips. Some of them were even serial-by-bit devices, which performed calculations a single bit at a time. The Intel 4004 chip took the integrated circuit down one step further by placing all the parts that made a computer think (i.e. central processing unit, memory, input and output controls) on one small chip. Programming intelligence into inanimate objects had now become possible**.** The 4004 was the world's first universal microprocessor. In the late 1960s, many scientists had discussed the possibility of a computer on a chip, but nearly everyone felt that integrated circuit technology was not yet ready to support such a chip. Intel's Ted Hoff felt differently; he was the first person to recognize that the new silicon-gated MOS technology might make a single-chip CPU (central processing unit) possible**.**

8-BIT MICROPROCESSORS:

Today, 8-bit microprocessors coexist with 16-bit microprocessors as the design standard. Although 16-bit chips provide higher performance computationally, 8-bit designs have more than adequate power for many applications—plus the advantage of lower cost. As originally design, most 16-bit microprocessors were limited to packages with a maximum of 40 to48 pins. This was not due to physical, but rather to economic, constraints: industrial tester of the time was generally limited to 40-pin DIPs. The ancestor of today's 8-bit microprocessors was the Intel 8008, introduced in 1972-1973. The 8008 was not intended to be a general-purpose microprocessor. IT was to be a CRT display controller for Data point. Taking into account all of its design inadequacies and its limited performance, the 8008 was an overwhelming success.

INTEL (8-BIT MICROPROCESSORS):

The 8080, designed as a successor to Intel's 8008, was the first powerful microprocessor introduced on the market. Several other microprocessors of similar performance were introduced on the market within a year after the 8080 appeared, and several additional powerful designs were introduced later. Technically, however, the 8080 long remained the most powerful product on the market. Furthermore, Intel was the first company to invest in the development of support chips and software for its products. This ensured the continued success of the 8080 because its performance was then sufficient for many applications. The early 8080 competitors were introduced with at least a nine-month delay and failed to dislodge it. The 8080 is still sold today thought It has been largely eclipsed by successor products—most notably the 8085 microprocessor. Today, the 8085 accounts for roughly one of every four 8-bit microprocessors sold.

1.2 MICROPROCESSOR ARCHITECTURE AND ITS OPERATION: Computer system consist primary of :-

1- Microprocessor.
2-Memory.
3-Input.
4-Output**.**

The internal logic design of the microprocessor called its"architecture", determine how and what various operations are performed by "MICROPROCESSOR".

Microprocessor architecture and its operations: The microprocessor is programmable logic device designed with register,flip-flop and timing elements.

All function performed by microprocessor can by classified in three general categories:-1- Microprocessor initiated operations.
2- Internal data operations.

3- Peripheral (or externally) initiated operations.

To performed these operations, microprocessor needs [logic circuit and control signals].

1- Microprocessor Initiated Operations:-

Primarily microprocessor performs **four** operations:-

a) Memory read (Reads data from memory).
b) Memory writes (Write data into memory).
c) I/O read (Accept data to output device).
d) I/O writes (Sends data to output device).

These operation are part of communication process.

Microprocessor performed these functions using sets of buses **[Data bus, Address bus, Control bus].**

Data bus: - is a group of 8 lines used for data flow, these lines are bidirectional from (00 – FF) $=2^8$ =256 numbers. The largest number = 1111 1111 = FF , thus 8085 Microprocessor is called 8bit Microprocessor.

Address bus: - is a group of 16 lines, identified as 0 – $_{15}$. This bus is unidirectional (bit flow in one direction) from Microprocessor to peripheral. Each memory location or peripheral identified with binary number called address. (2^{16} =65536=64K).

Control bus: - the control is comprised of various single lines that carry synchronization signals.

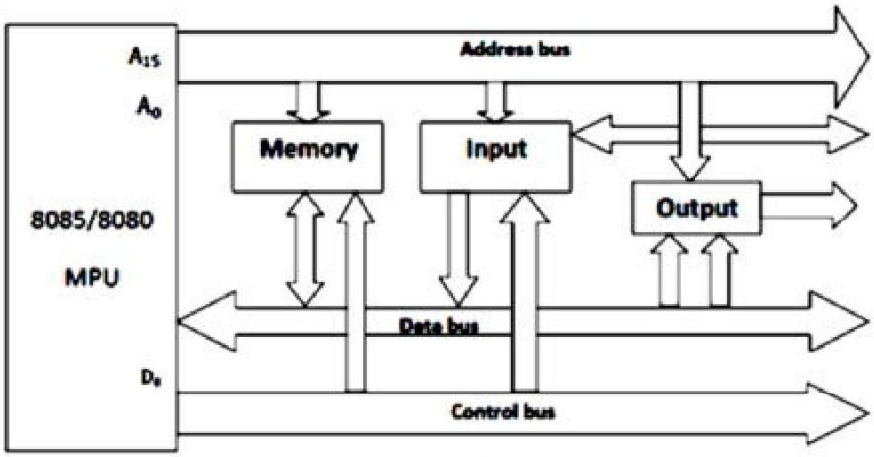


Fig. 1.1 The 8085 Bus System

The microprocessor needs to perform the followingsteps:-

i) Identify the peripheral (memory location).
ii) Transfer data.
iii) Provide timing or synchronization signals.

2- Internal Data Operations:-

The internal architecture of the 8085/8080A microprocessor determines how and what operation can be performed with the data. These operations are:-

1- Store 8-bit data.

2- Performed arithmetic and logical operations.

3- Test for conditions.

4- Sequence the execution of instructions.

5- Store data temporarily during execution in the defined R/W memory locations called the stack. To perform these operations the Microprocessor requires:-

a) Registers.

b) An arithmetic logic unit (ALU) & control logic.

c) Internal buses (paths for information flow).

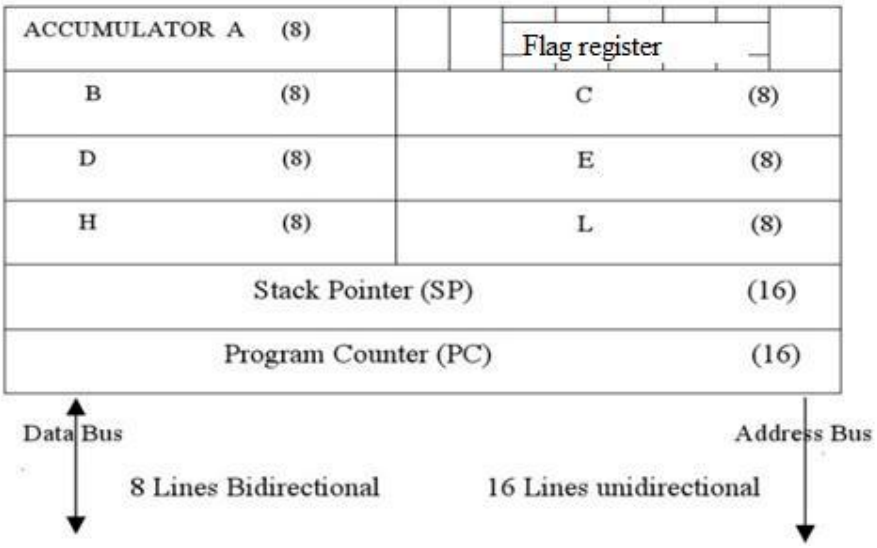


Fig1.2 : The 8085 Programmable Register

3- Peripheral or Externally Initiated Operations:-

External devices (or signals) can initiate the following operation for which individual pins on Microprocessor chip are assigned: **Reset, Interrupt, Ready, Hold.**

A) Reset: when reset is activated all internal operations are suspended and the program counter is cleared.

B) Interrupt: the Microprocessor can be interrupted from normal execution and asked to execute other instructions called **"service routine"** (emergency), Microprocessor resumes its operation after that.

C) Ready: 8085 has pin called ready, if the signal is low Microprocessor enters into wait state, this signal used to synchronized slower peripherals with Microprocessor.

D) Hold: when hold pin activated by external signal Microprocessor relinquishes control buses and allows the external peripheral to use the. For example: Hold signal is used in direct memory

access data transfer.

1.3 MEMORY, INPUT AND OUTPUT: Memory is an essential component of a microprocessor system; it stores binary information. The memory is made up of semiconductor material used to store the programs and data. The types of memory is, Primary or main memory and Secondary memory.

Primary memory: RAM and ROM are examples of this type of memory. Microprocessor uses it in storing a program temporarily (commonly called loading) and executing a program. Hence the speed of this type of memory should be fast.

Secondary memory: These are used for bulk storage of data and information. The main examples include Floppy, Hard Disk, CD-ROM, Magnetic Tape etc. Slower and Sequential Access Nature.non-volatile nature.

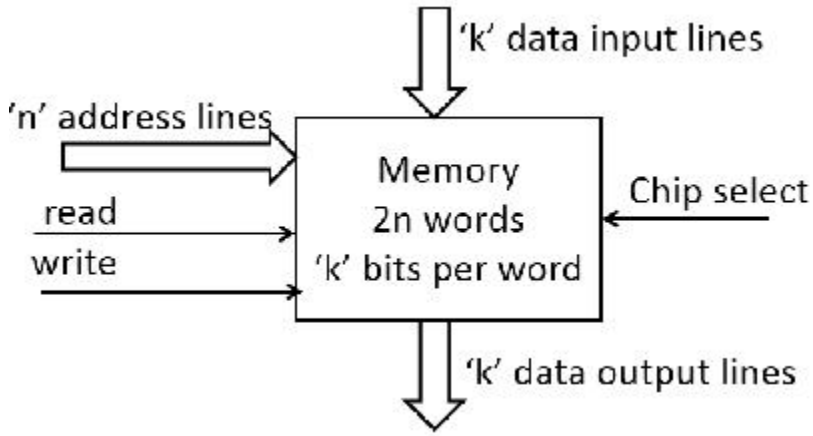


Fig. 1.3 Memory chip

The Basic Memory Element: The basic memory element is similar to a D latch.This latch has an input where the data comes in. It has an enable input and an output on which data comes out.

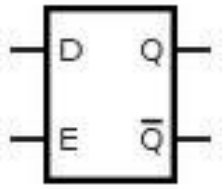


Fig. 1.4 D Latch

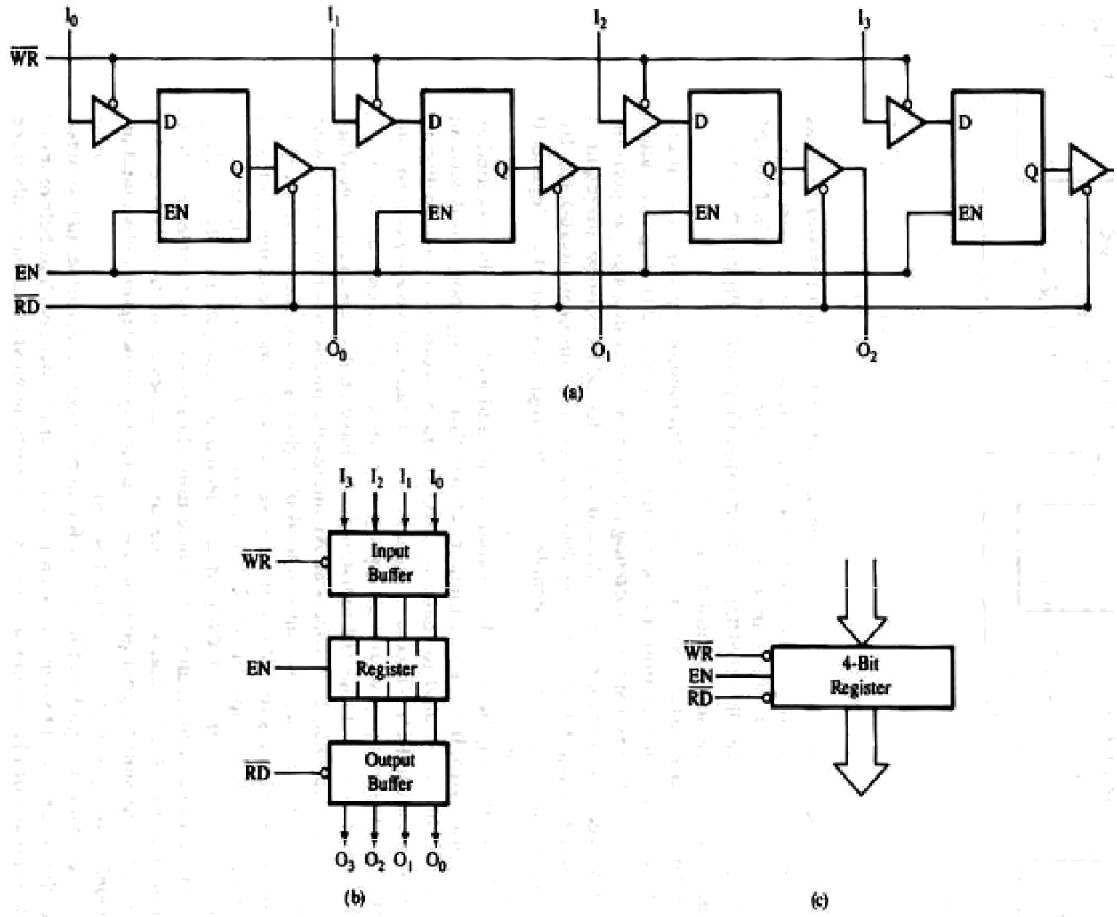


Fig.1.5: D latch as a 4-bit storage element

Address Decoding and Memory Mapping: Memory address decoding is nothing but to assign an address for each location in the memory chip. The data stored in the memory is accessed by specifying its address. Memory address can be decoded in two ways:

i) Absolute or Fully decoding and ii) Linear Select or Partial decoding

There are many advantages in absolute address decoding.

i) Each memory location has only one address, there is no duplication in the address
ii) Memory can be placed contiguously in the address space of the microprocessor
iii) Future expansion can be made easily without disturbing the existing circuitry

There are few disadvantages in this method

i) Extra decoders are necessary

ii) Some delay will be produced by these extra decoders.

The main advantage of linear select decoding is its simplified decoding circuit.This reduces the hardware design cost. But there are many disadvantages in this decoding.

i) Multiple addresses are provided for the same location

ii) Complete memory space of the microprocessor is not efficiently used

iii) Adding or interfacing ICs with already existing circuitry is difficult.

Absolute Address Decoding: The 8085 microprocessor has 16 address lines. Therefore it can access 2^{16} locations in the physical memory. If all these lines are connected to a single memory device, it will decode these 16 address lines internally and produces 216 different addresses from 0000H to FFFFH so that each location in the memory will have a unique address.

A_{15} A_{14} A_{13} A_{12}	A_{11} A_{10} A_9 A_8	A_7 A_6 A_5 A_4	A_3 A_2 A_1 A_0	Hex Address
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0000H
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0001H
0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0002H
- - -	- - -	- - -	- - -	- - -
- - -	- - -	- - -	- - -	- - -
1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 0	FFFEH
1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 0	FFFFH

Fig. 1.6 Memory Address

Above diagram shows the various memory addresses used in Microprocessor. If more than one chips are used then some logic must be used to select one particular chip. This is done with the help of decoder.

74LS138 address decoder to generate the chip select signals for eachmemory block. In this decoder when the address lines A**13**, A**14** and A**15** are 000, theoutput line**Y0** will be activated as shown in Fig 1.7. This in turn selects the firstmemory block. Similarly when these lines are 001 (C=0, B=0 and A=1) Y1 will beactivated and the second memory block will be selected.

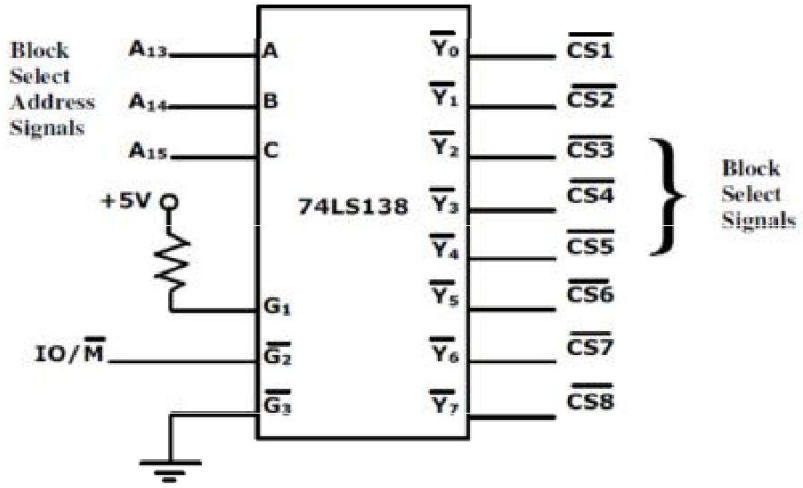


Fig 1.7: Memory block decoder

In this type of memory interfacing, all the address lines (A0 to A15) have beenused. Each

location in the memory will have a single address. This type of addressdecoding is called as absolute or fully decoded addressing.

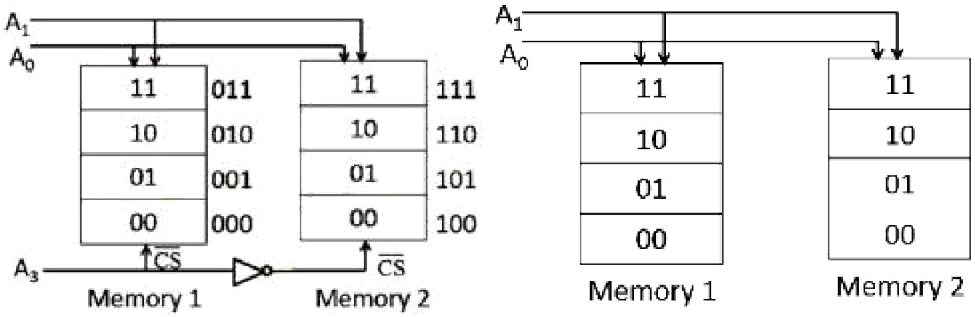


Fig. 1.8: Role of CS signal

According to the value of Ao and A1 , any one register will be selected and to select one memory chip we need one chip select signal CS signal as shown in the next diagram.

If CS' is '0'memory 1 will be selected else memory2 will be selected. And the complete picture of the interfacing is shown below.

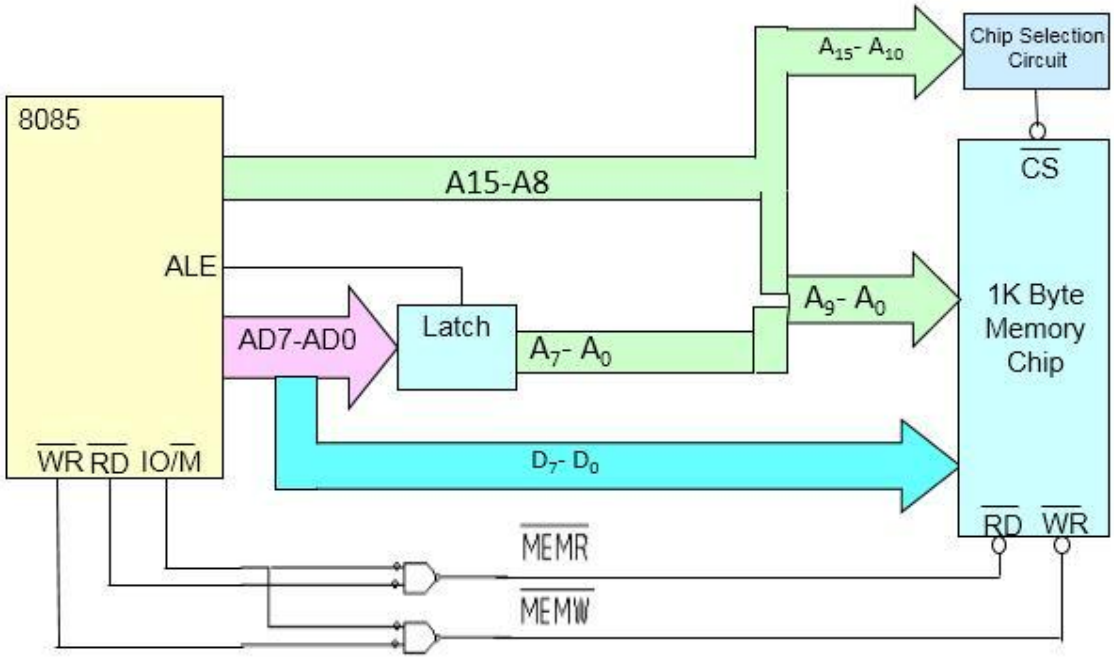


Fig. 1.9: The complete interfacing diagram

The simple view of RAM is that it is made up of registers that are made up of flip-flops (or memory elements). The number of flip-flops in a "memory register" determines the size of the memory word.ROM on the other hand uses diodes instead of the flip-flops to permanently hold the information. For the microprocessor to access (Read or Write) information in memory (RAM or ROM), it needs to do the following:

Select the right memory chip (using part of the address bus). Identify the memory location (using the rest of the address bus). Access the data (using the data bus).

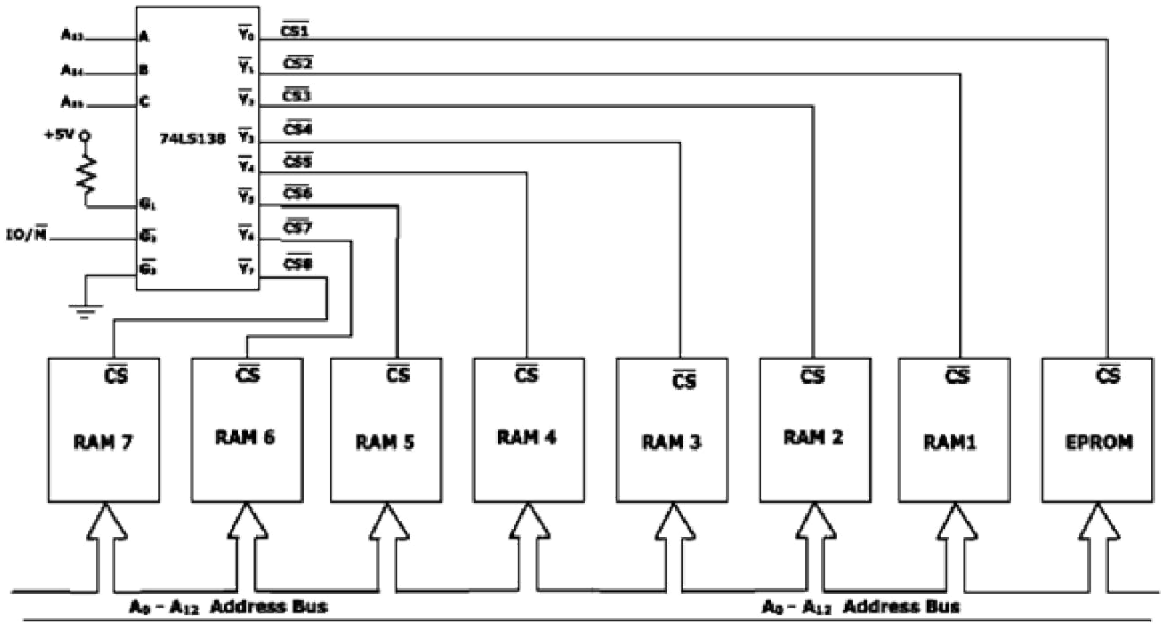


Fig. 1.10 Memory Interface Diagram

Tri-State Buffers: An important circuit element that is used extensively in memory. This buffer is a logic circuit that has three states: Logic 0, logic1, and high impedance. When this circuit is in high impedance mode it looks as if it is disconnected from the output completely. This circuit has two inputs and one output. The first input behaves like the normal input for the circuit. The second input is an “enable”. If it is set high, the output follows the proper circuit behaviour. If it is set low, the output looks like a wire connected to nothing.

Input /Output Devices: Parallel Interfacing: There are two ways to interface 8085 with I/O devices in parallel data transfer mode: Memory Mapped IO and IO mapped IO.

Memory mapped I/O: It considers them like any other memory location. They are assigned a 16-bit address within the address range of the 8085.The exchange of data with these devices follows the transfer of data with memory. The user uses the same instructions used for memory.

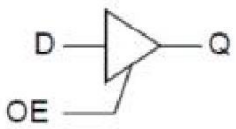
I/O mapped I/O: It treats them separately from memory: I/O devices are assigned a “port number” within the 8-bit address range of 00H to FFH. The user in this case would access these devices using the IN and OUT instructions only.

IO mapped IO V/s Memory Mapped IO:

Memory Mapped IO	IO mapped IO
• IO is treated as memory. • 16-bit addressing. • More Decoder Hardware. • Can address 2^{16}=64k locations. • Less memory is available. • Memory Instructions are used. • Memory control signals are used. • Arithmetic and logic operations can be performed on data. • Data transfer b/w register and IO.	• IO is treated IO. • 8- bit addressing. • Less Decoder Hardware. • Can address 2^{8}=256 locations. • Whole memory address space is available. • Special Instructions are used like IN, OUT. • Special control signals are used. • Arithmetic and logic operations cannot be performed on data. • Data transfer b/w accumulator and IO.

1.4 LOGIC DEVICES FOR INTERFACING: Several types of interfacing devices are necessary to interconnect the components of a bus oriented system. Tristate logic devices are essential to proper functioning of bus oriented system.

Tri state Devices: A tri state (bus driver) device is a device that can be active low, active high, or floating. The use of a tri state device is that several of them can be connected to a single bus line and, so long as only one of them is non-floating, the bus line can be driven by multiple senders. The data bus is most often implemented with tri state drivers.



OE	D	Q
H	L	L
H	H	H
L	x	hi-Z

Fig.1.11 Tri state device

The data will be passed to the output terminal whenever the OE terminal is activated, else the device will be in high impedance state.

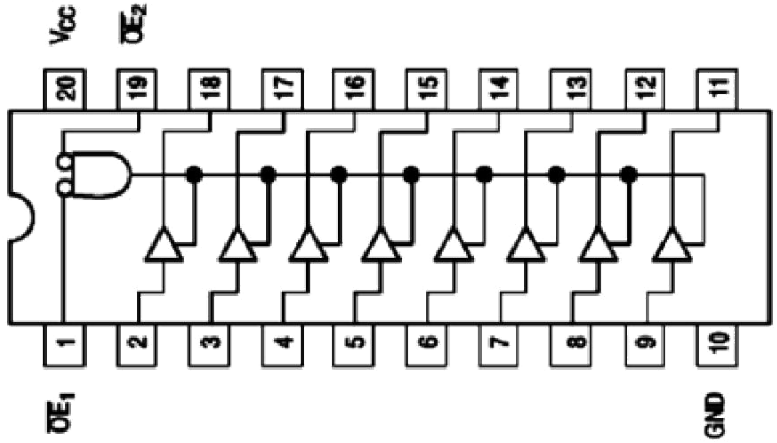


Fig.1.12 Octal 3 state Buffer

It is common to use an octal 3-state buffer as shown in fig. 1.12 to create a byte-wide input port. The '541 has dual active-low enable inputs in order to pass its D inputs from input devices to their respective Q outputs and onto the system data bus. OE1 could connect to the address decoder for this input port while OE2 could connect to an active-low READ strobe. This READ strobe requirement is imperative so as to keep the output drivers disabled and avoid the dreaded "self destruct state" due to bus contention. Bus contention is the result of more than a single driver on a shared bus line being active at the same time and potentially driving a bus line to opposing logic levels. Such would be the case if the READ strobe were ignored during a CPU write operation.

Bidirectional Ports: The octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE)\ input can disable the device so that the buses are effectively isolated.

Features

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce dc Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

IC used for this purpose is 74LS245 and the pin diagram is shown below:

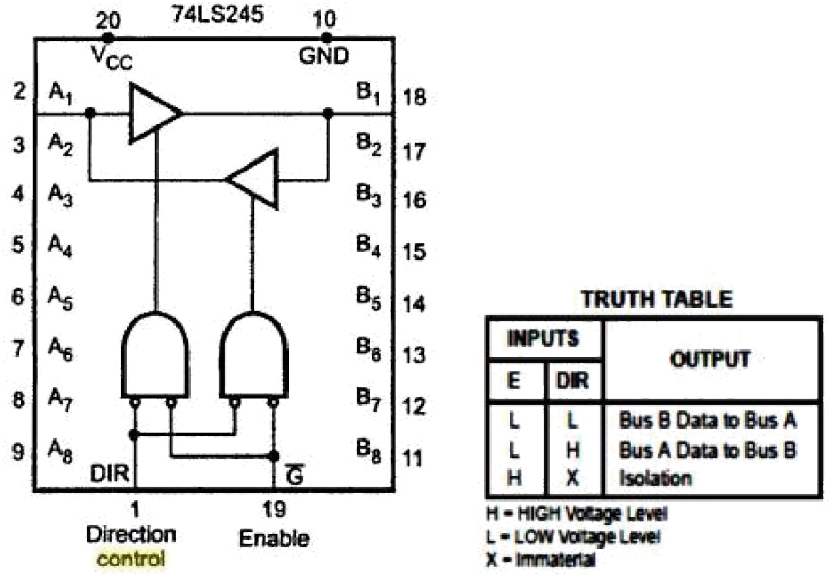


Fig. 1.13 Logic diagram and function Table of 74LS245 Bidirectional buffer

D-Latch: Latch and flip flop are the most common logic devices that are used to store one bit data. A simple latch has two stable logic states. The latch maintains its states indefinitely until an input pulse called a trigger is received. If a trigger is received, the latch outputs change states according to defined rules, and remain in those states until another trigger is received. Latches can be interconnected to form more sophisticated circuits that function in memory chips and microprocessors.

An octal latch can hold onto the data at its inputs before transmitting the data to its outputs. This ability is useful in applications where a number of devices share a single data bus, because it allows the processor to store data, go onto other operations that require the bus, and return to the stored data later if the need arises.

And the group of latch or flip flop is known as register. Commonly used IC is 74LS373. Pin diagram is shown below.

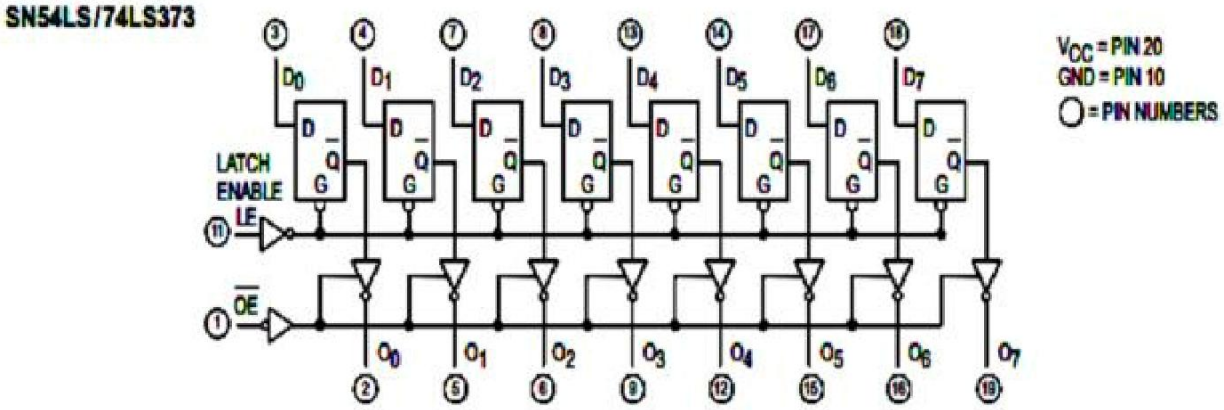


Fig1.14 Pin Diagram of 74LS373

1.5 8085 MPU: The microprocessor is a semiconductor device (Integrated Circuit) manufactured by the VLSI (VeryLarge Scale Integration) technique. It includes the ALU, register arrays and control circuit on asingle chip. To perform a function or useful task we have to form a system by using microprocessor as a CPU and interfacing memory, input and output devices to it. A system designed using a microprocessor as its CPU is called a microcomputer. The Microprocessor based system (single board microcomputer) consists of microprocessor as CPU, semiconductor memories like EPROM and RAM, input device, output device and interfacing devices. The memories, input device, output device and interfacing devices are called peripherals. The popular input devices are keyboard and floppy disk and the output devices are printer, LED/LCD displays, CRT monitor, etc

The main features of 8085 **µ**p are:

• It is a 8 bit microprocessor.

• It is manufactured with N-MOS technology.

• It has 16-bit address bus and hence can address up to 2^{16} = 65536 bytes (64KB) memory locations through A0-A15

• The first 8 lines of address bus and 8 lines of data bus are multiplexed AD0 – AD7

• Data bus is a group of 8 lines D0 – D7

• It supports external interrupt request. .

• A 16 bit program counter (PC)

• A 16 bit stack pointer (SP)

• Six 8-bit general purpose register arranged in pairs: BC, DE, HL.

• It requires a signal +5V power supply and operates at 3.2 MHZ single phase clock.

• It is enclosed with 40 pins DIP (Dual in line package).

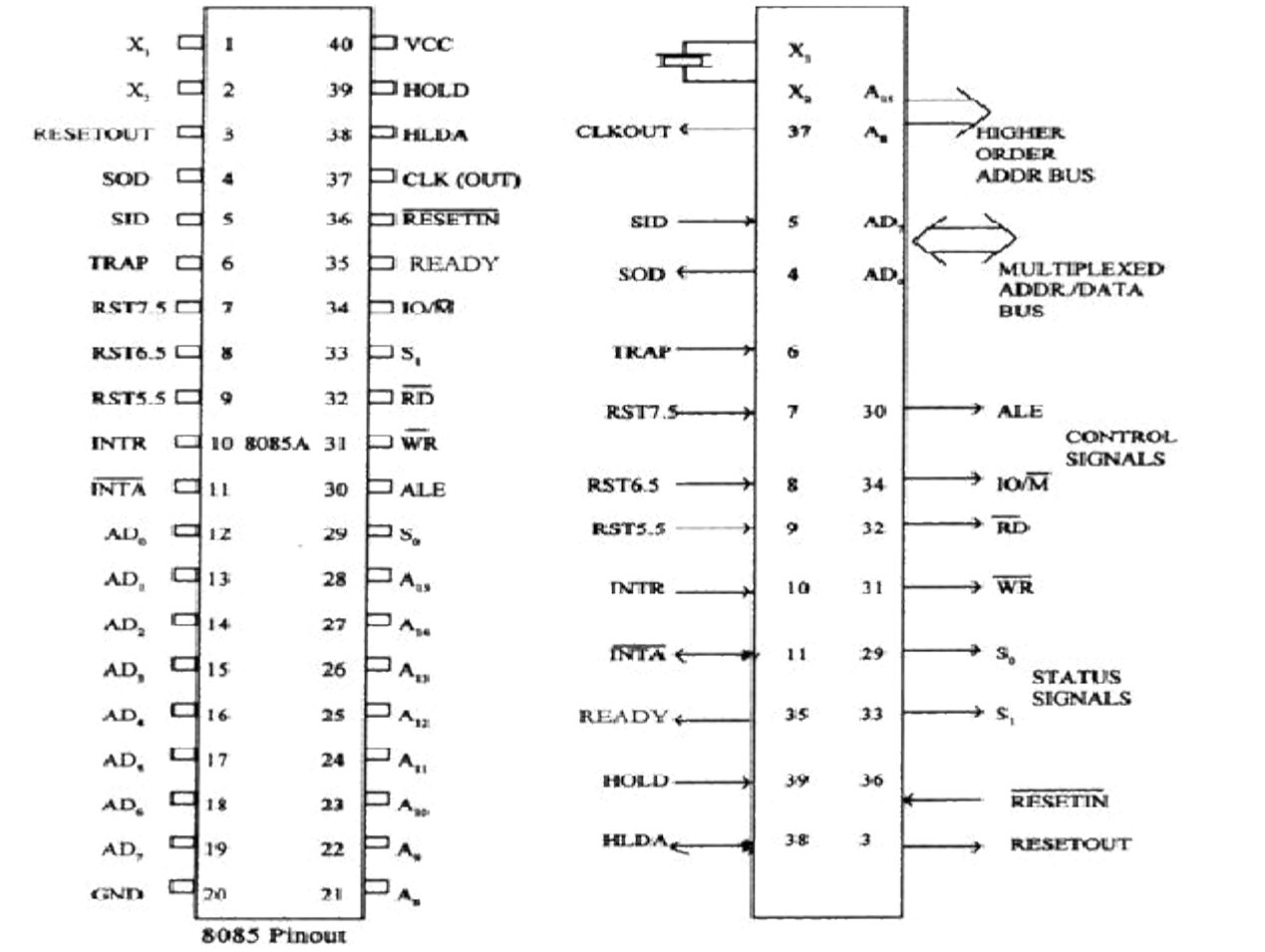
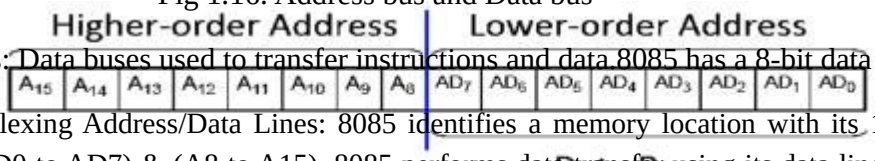


Fig.1.15 Pin diagram of 8085 Microprocessor

System Bus: Typical system uses a number of busses, collection of wires, which transmit binary numbers, one bit per wire. A typical microprocessor communicates with memory and other devices (input and output) using three busses: Address Bus, Data Bus and Control Bus.

Address Bus :One wire for each bit, therefore 16 bits = 16 wires. Binary number carried alerts memory to 'open' the designated box. Data (binary) can then be put in or taken out. The Address Bus consists of 16 wires, therefore 16 bits. Its "width" is 16 bits. A 16 bit binary number allows 2^{16} different numbers, or 32000 different numbers, ie 0000000000000000 up to 1111111111111111. Because memory consists of boxes, each with a unique address, the size of the address bus determines the size of memory, which can be used. To communicate with memory the microprocessor sends an address on the address bus, eg 0000000000000011 (3 in decimal), to the memory. The memory the selects box number 3 for reading or writing data. Address bus is unidirectional, ie numbers only sent from microprocessor to memory, not other way. These address lines are split into two parts A_{15}-A_8 are unidirectional and AD_0-AD_7.

Fig 1.16: Address bus and Data bus



Data Bus: Data buses used to transfer instructions and data.8085 has a 8-bit data bus

Demultiplexing Address/Data Lines: 8085 identifies a memory location with its 16 address lines, (AD0 to AD7) & (A8 to A15) .8085 performs data transfer using its data lines, AD0 to AD7.Lower order address bus & Data bus are multiplexed on same lines i.e. AD0 to AD7.Demultiplexing refers to separating Address & Data signals for read/write operations.

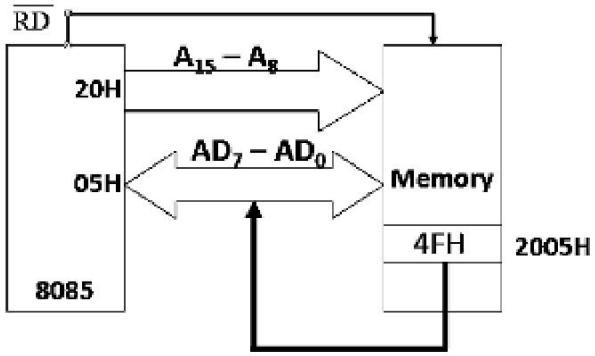


Fig. 1.17 Need for Demultiplexing

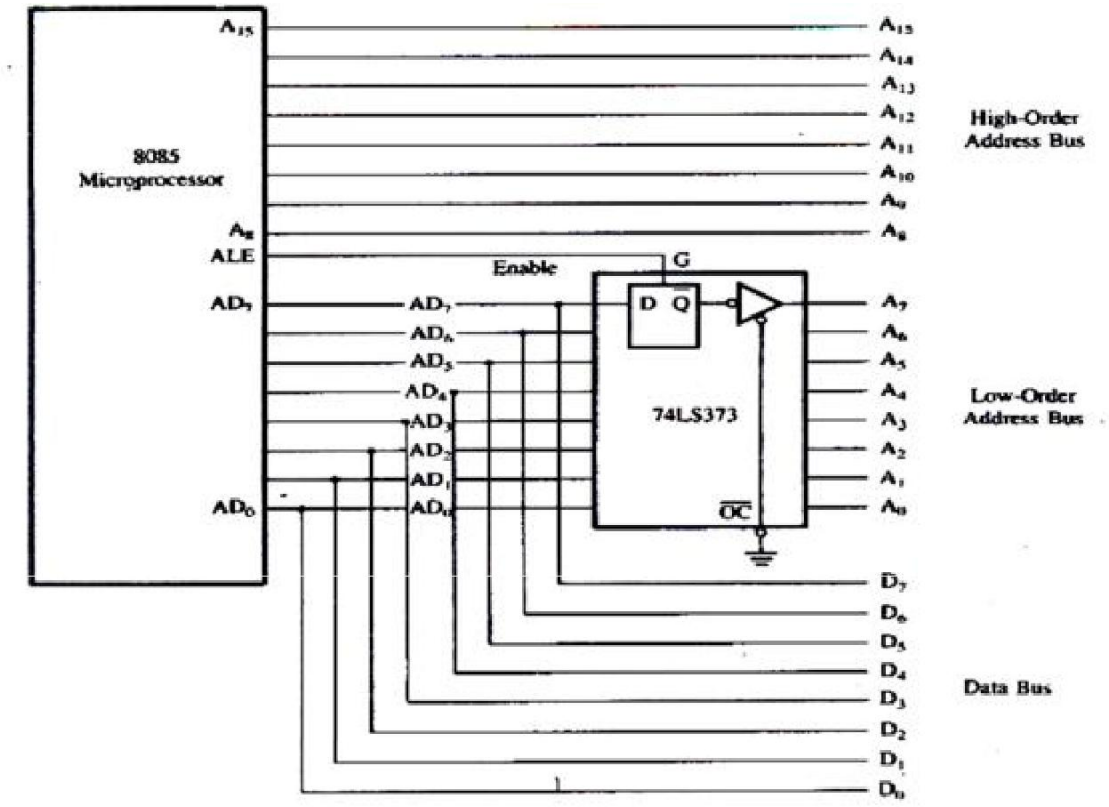


Fig 1.17: Demultiplexing data lines from address lines

Control and Status signal: This group of signals includes two control signals (RD and

WR), three status signals (IO/M, S1 and S0) to identify the nature of the operation. These signals are as follows:

ALE (Address Latch Enable): This is a positive going pulse generated every time the 8085 begins an operation (machine cycle); it indicates that the bits on AD7-AD0 are address bits. This signal is used primarily to latch the low-order address from the multiplexed bus and generate a separate set of eight address lines, A7-A0.

RD (Read): This is a Read control signal (Active Low). This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.

WR (Write): This is a write control signal (Active Low). This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.

IO/M: This is a status signal used to differentiate between I/O and memory operations. When it is high, it indicates an I/O operation: when it is low, it indicates a memory operation. This signal is combined with RD (read) and WR (Write) to generate I/O and memory control signals.

S1 and S0: These status signals, similar to IO/M, can be identify various operations, but they are rarely used in small systems.

Power Supply and Clock frequency: The power supply and frequency that are used in 8085 Microprocessor are as follow:

Vcc: +5V power supply.

Vss: Ground reference.

X1, X2: A crystal is connected at these two pins. The frequency is internally divided by two; therefore, to operate a system at a 3 MHz, the crystal should have a frequency of 6 MHz .

CLK (OUT)-Clock Output: This signal can be used as the system clock for other devices.

Pin description: Properties : Single + 5V Supply , 4 Vectored Interrupts (One is Non Maskable) , Serial In/Serial Out Port , Decimal, Binary, and Double Precision Arithmetic . Direct Addressing Capability to 64K bytes of memory

The Intel 8085A is a new generation, complete 8 bit parallel central processing unit (CPU). The 8085A uses a multiplexed data bus. The address is split between the 8bit address bus and the 8bit data bus. Figures are at the end of the document.

Pin Description : The following describes the function of each pin:

A6 - A1s (Output 3 State)

Address Bus; The most significant 8 bits of the memory address or the 8 bits of the I/0 address,3 stated during Hold and Halt modes.

AD0 - 7 (Input/Output 3state) :Multiplexed Address/Data Bus; Lower 8 bits of the memory address (or I/0 address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles. 3 stated during Hold and Halt modes.

ALE (Output) : Address Latch Enable: It occurs during the first clock cycle of a machine state and enables the address to get latched into the on chip latch of peripherals. The falling edge of ALE is

set to guarantee setup and hold times for the address information. ALE can also be used to strobe the status information. ALE is never 3stated.

SO, S1 (Output)

Data Bus Status. Encoded status of the bus cycle:

S1	S0	Operation
O	O	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S1 can be used as an advanced R/W status.

RD (Output 3state) : READ; indicates the selected memory or 1/0 device is to be read and that the Data Bus is available for the data transfer.

WR (Output 3state) : WRITE; indicates the data on the Data Bus is to be written into the selected memory or 1/0 location. Data is set up at the trailing edge of WR. 3stated during Hold and Halt modes.

READY (Input) :If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

HOLD (Input) :HOLD; indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request. will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue.

The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, RD, WR, and IO/M lines are 3stated.

HLDA (Output) :HOLD ACKNOWLEDGE; indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes low.

INTR (Input) :INTERRUPT REQUEST; is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

INTA (Output) :INTERRUPT ACKNOWLEDGE; is used instead of (and has the same timing as) RD during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.

RST 5.5

RST 6.5 - (Inputs)

RST 7.5

RESTART INTERRUPTS; These three inputs have the same timing as I NTR except they cause an internal RESTART to be automatically inserted. RST 7.5 ~~ Highest Priority

RST 6.5 RST 5.5 o Lowest Priority .The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR.

TRAP (Input): Trap interrupt is a nonmaskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

RESET IN (Input) :Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flipflops. None of the other flags or registers (except the instruction register) are affected The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output) :Indicates CPlJ is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X1, X2 (Input) :Crystal or R/C network connections to set the internal clock generator X1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

CLK (Output) :Clock Output for use as a system clock when a crystal or R/ C network is used as an input to the CPU. The period of CLK is twice the X1, X2 input period.

IO/M (Output) :IO/M indicates whether the Read/Write is to memory or l/O Tristated during Hold and Halt modes.

SID (Input) :Serial input data line The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (output) :Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

Generating Control signals: The Mp provides RD and WR signals to initiate read and write cycle. Because these signals are used both for reading / writing memory or reading writing an input/output device, it is necessary to generate separate read and write signals for memory and I/O devices. 8085 provides IO/M signal to indicate that initiated cycle is for I/O device or for memory device. Using IO/M signal along with RD and WR, it is possible to generate four signals shown below.

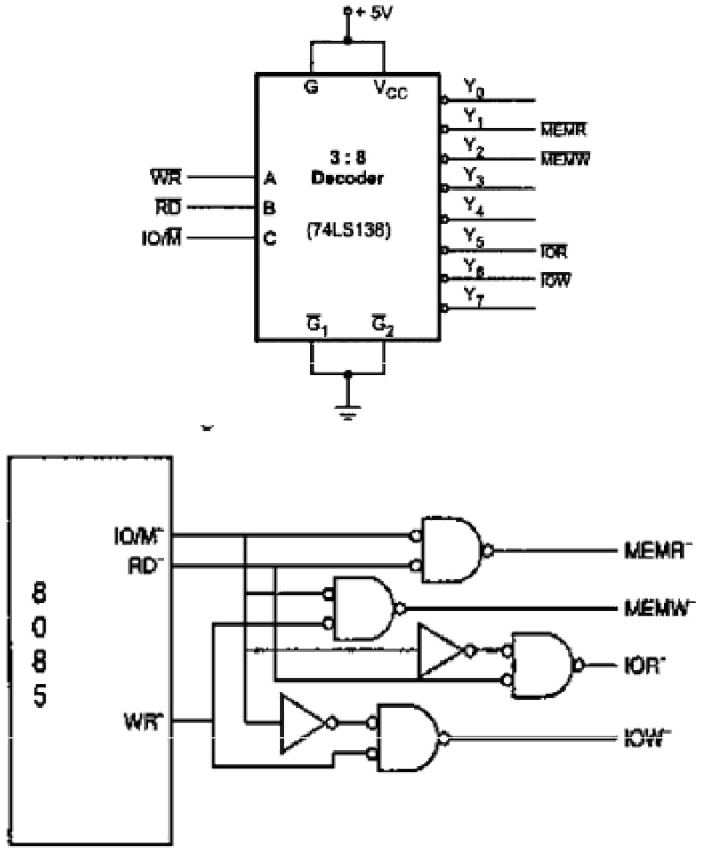


Fig.1.18 : Generating Control Signals

Generationof control signals:

Table 1.2: Generation of control signals

$IO/\overline{M}$	$\overline{RD}$	$\overline{WR}$	$\overline{MEMR}$ $\overline{RD} + IO/\overline{M}$	$\overline{MEMW}$ $\overline{WR} + IO/\overline{M}$	$\overline{IOR}$ $\overline{RD} + IO/\overline{M}$	$\overline{IOW}$ $\overline{WR} + IO/\overline{M}$
0	0	0	Condition never exists, because $\overline{RD}$ and $\overline{WR}$ signals does not go low simultaneously			
0	0	1	0	1	1	1
0	1	0	1	0	1	1
0	1	1	1	1	1	1
1	0	0	Condition never exists, because $\overline{RD}$ and $\overline{WR}$ signals does not go low simultaneously			
1	0	1	1	1	0	1
1	1	0	1	1	1	0
1	1	1	1	1	1	1