**LOGIC FAMILIES**

**Main Logic Families: -** Most digital system are designed by combining various logic functions. All these logic circuits are available in IC modules and are divided into many “families”. Each family is classified by abbreviations which indicate the type of logic circuit used. For example, RTL means resistor-transistor logic. We will discuss the following seven transistor logic families although the first two are, at preset, of historic interest only.

1. **Resistance-transistor logic (RTL) --** it was the first family group of logic circuits to be developed and packaged in IC form in *early*1960s;
2. **Direct Coupled Transistor Logic (DCTL)**
3. **Diode-transistor logic (DLT):-** it followed RTL in *late* 1960s;
4. **transistor**-**transistor logic(TTL):-** or **(T2L): -** was introduced in the early 1970s;
5. **Schottky TTL (74LS00):**- was introduced to improve the speed of TTL.
6. **Emitter**-coupled logic (ECL)-- it is the fastest logic line currently available;
7. **integrated**- **injection logic(I2L):-** it is one of the latest of the bipolar types of logic;
8. **PMOS and NMOS logic.**
9. **Complementary metal**-oxide semiconductor (CMOS):- it has the lowest power dissipation of the currently- available logic circuits.

The various logic families discussed above possess different characteristics as detailed below.

**Saturated and Non-saturated Logic Circuits**:-

Those logic circuit in which transistors are driven into saturation are called **saturated** logic circuits or simply **saturated logic**. Those circuits which avoid saturation of their transistors are designated **non-saturated logic.** Those circuits which avoid saturation of their transistors are designated non-saturated logic.

The disadvantage of saturated logic is the delay that occurs when the transistor is brought out of saturation. When a transistor is saturated, its base is flooded with carriers. Even when base voltage is switched off, the base remains flooded for some time till all carriers leave it. The time required by the carriers to leave the base is called saturation delay time (ts). Obviously, saturated logic circuits have low switching speeds whereas non-saturated type are much faster. TTL is the example of a saturated logic whereas ECL represents a non-saturated logic.

**Characteristics of Logic Families**:-

The logic families possess different characteristics because of which one may prove to be the best suited for a particular job. For example, in a certain system, speed may be the main requirement, whereas in another system minimum power dissipation might be the overriding consideration. The different characteristics of a logic family are as under:

1. Speed of operation (propagation delay) (ns). 2. Fan-in 3. Fan-out 4. Noise immunity 5. Power dissipation.

**Speed** of a logic gate is the time that elapses between the application of a signal to an input terminal and the resulting change in logical state at the output terminal. It takes into account the transition times (rise and fall times of a pulse) and propagation delays. Both these times increase at the loading is increased. The more inputs are attached to the output of a logic gate, the more load has to be handled by that output.

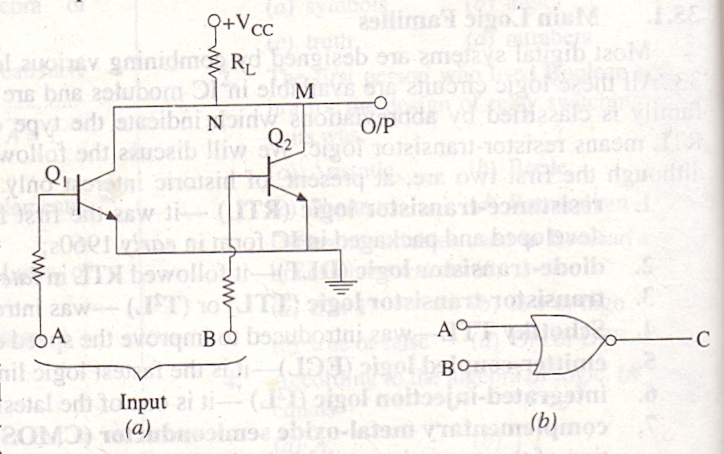
The **fan-in** of a logic gate is the number of inputs (coming from similar circuits) the logic gate can handle properly.

The **fan-out** of a logic gate is the maximum number of similar circuits that this gate can drive reliably. For example, if a gate has a fan-out of 8, this means that it can drive 8 units connected to its output without its output voltage falling outside the limits at which the logic levels 1 and 0 are specified.

Noise immunity is represented by the maximum induced noise voltage a logic circuit can withstand without a false change in its output state. It is also called **noise margin**. Too much nose voltage induced by stray electric and magnetic fields can lead to false triggering of logic levels in the circuit. Higher the noise margin, better the logic circuit.

**Power is dissipated** in a circuit as it switches from one state to another and within all current-carrying resistors. Power dissipation of a gate should be as small as possible.

**RTL Circuit:-** It is a saturated logic. It uses only transistors and resistor and circuit elements and resistors in the input to each base. This family is based on the NOR circuit shown in Fig.1. All other members of the family are made up of NOR calls or variations on them.



**Figure 1.**

**Circuit Operation**

We will assume ideal transistors. When both inputs A and B are 0V (or logic 0), both transistors are turned OFF, hence point M goes to +VCC so that output is logic1.

If either or both input terminal are at + VCC i.e., are high (or logic 1), one or both transistors would be fully turned ON (i.e., saturate) thereby reducing the voltage of point N to almost 0 V. Hence, output would be at logic 0.

It is seen that the output is at as logic 1 *only when both inputs are at logic 0* -- the NOR logic function as shown in Fig.1 (b).

The RTL family has the following characteristics:-

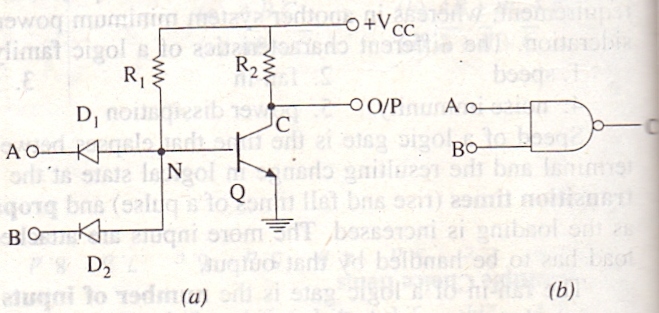
1. Relatively slow speed. 2. Low fan-out of 6 and a fan-in of 4,

3. Poor noise immunity, 4. Expensive since resistors are required to be fabricated,

5. Cannot operate at speeds above 4 MHz

**DTL Circuit**

It is a saturated logic because transistors operate between cut-off and saturation. It was the next family to be introduced after RTL. It consists of diodes, resistors and transistors. The basic gate of this family performs NAND function. As shown in Fig. 2 (a), the circuit basically consists of a diode AND gate followed by a transistor inverter which leads to a NAND gate.



**Figure 2.**

**Circuit Operation:-**

1. When both D1and D2 have positive voltage applied to them (logic1), neither conducts and Q is turned ON by the current provided by VCC through R1. Since Q becomes saturated, point C is brought to 0 V (logic 0). Hence, output goes logic 0.
2. If either or both inputs are at 0 V (logic0), the associated diode will conduct driving point N to ground i.e., 0 V. Since there is no base voltage for Q. it will be cut OFF thereby driving point C and hence output to VCC i.e., logic 1.

**NAND gate:-**

The DTL family is characterized by

1. Relatively lower speed, 2. Comparatively better noise immunity

3. Delay of 30 ns, 4. A fan-in of 8,

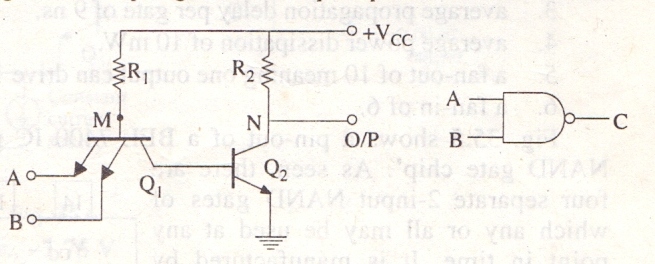
5. A fan-out of 5.

**TTL Circuit**

It is a *saturated* logic. It is the most widely used circuit line since early 1970s because of its speed, good fan-in and fan-out and easy interface with other digital circuitry. The unique feature of this circuit is that it uses multiple-emitter transistor at the input which replaces the input diodes of the DTL. The number of emitters is equal to the desired fan-in of the circuit. Since a multi-emitter transistor is smaller in area than the diodes it replaces, the yield from a wafer is increased. Moreover, smaller area results in a lower *capacitance* to the subscribe, thereby reducing circuit rise and fall times and hence increasing its speed. The family contains a very wide selection of circuit modules ranging from simple gates and flip-flops in SSI circuit series through various ‘registers’ in computers in MSI circuit series to micro-processor bit-slice chips in the LSI series.

**Basic Circuit**

The basic circuit of the TTL family is the NAND gate cell shown in Fig.3. However at present, NOR, OR and NND gate configurations have also been added to the series.



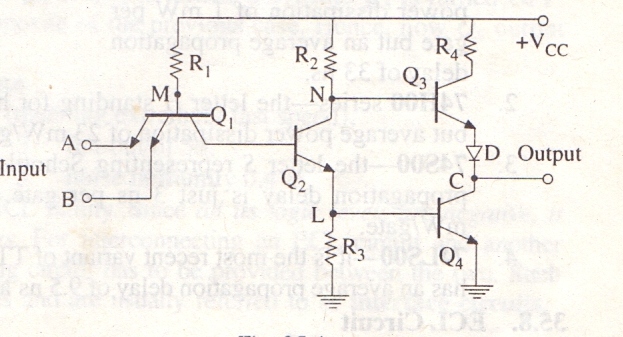
**Figure 3.**

**Circuit Operation**

1. If both inputs A and B are high (logic1). E/B junction of Q1 is reverse-biased so that it has no emitter current. Hence, Q1 is OFF. However, its C/B junction is forward-biased supplying base current to Q2 from VCC via R1. As a result, transistor Q2 is turned fully on (i.e., it becomes saturated) driving point N to 0 V. Hence, output is at logic 0.
2. When either or both inputs are at 0 V (logic 0), the associated E/B junction becomes forward-biased. The value of R1 is so selected as to ensure that Q1 is turned fully ON. The voltage at point M falls to 0 V with the result that base current for Q2 is reduced to zero. Hence, Q2 is cut OFF driving point N and the output to logic 1.

**Totem pole out put**

The basic circuit of Fig.3 is never used in practice. Its modified version with an added output stage is in common use (Fig. 4). The extra output stage is often known as totem-pole stage because the three output component Q3, Q4 and D are stacked, one on top of the other in the manner of a to- tem-pole. The circuit action is as follows:

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**Figure 4.**

1. **When Input is High**

In this case, the two input terminals have positive voltage (logic 1). The E/B junction is reverse-biased because of which there is no emitter current. Hence, Q1 is OFF. Since C/B junction of Q1 is forward-biased, base current of Q2 flows from VCC through R1. Hence, Q2 turned ON. As a result, potential of point N falls so much that Q3 is turned OFF. At the same time, Q4 is turned ON by the voltage drop across R3. Now, when Q4 is ON, its collector potential (i.e., potential of point C ) is nearly that of its emitter. Hence, output is low i.e., at logic 0.

In short, when inputs are at logic 1. Q1 is OFF, Q2 is ON, Q3 is OFF and Q4 is ON because of which output becomes logic 0

1. **When Input is Low**

If any of the two input of both are low (logic 0) Q1 turned On and potential of it collector (point M) falls. Hence, Q2 is turned OFF, grounding its emitter and the base of Q4 so that Q4 is also turned OFF.

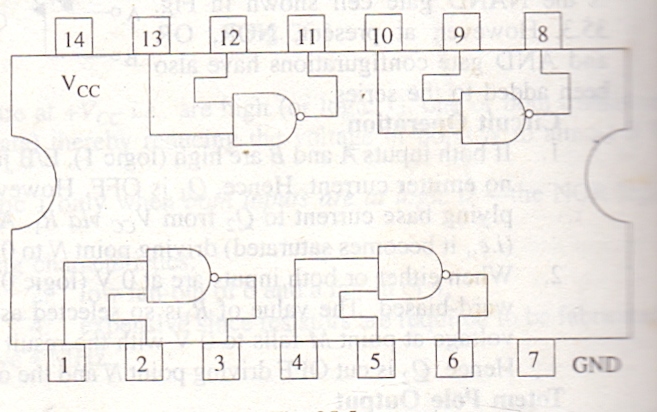
Since N is at VCC it turns Q3 On. The potential of point C is VCC minus drop in R4, Q3 and D. Since these drops do not amount too much. Output is at logic 1.

It may be noted that when *even-numbered transistors are ON, the odd-numbered ones are OFF and vice-versa.*

The function of diode D in Fig. 4 is to prevent both Q3 and Q4 from being turned ON simultaneously. If both were to be ON at the same time, they world offer low impedance to the supply which will draw excessive current and produce large noise ‘spikes’ output. It may also be noted that the addition of a pair of totem pole transistor increases the operating speed and output current capability of this circuit. The standard TTL family has

1. Greater speed than DTL,
2. Less noise immunity (0.4V),
3. Average propagation delay per gate of 9ns,
4. Average power dissipation of 10 mW,
5. A fan-out of 10 meaning one output can drive 10 other TTL inputs,
6. A fan-in of 6.

Fig shows a pin-out of a BEL 7400 IC referred to as ‘quad (quadrupole) 2-input NAND gate chip’. As seen, there are four separate 2-input NAND gates of which any or all may be used at any point in time. It is manufactured by Bharat Electronics Ltd., (BEL) Bangalore, India.



**TTL Subfamilies**

**TTL** has several subfamilies having deferent speed and power dissipation characteristics as detail below:

1. **74L00** series- the letter L standing for low power consumption. It has an average power dissipation of 1 mW per gate but an average propagation delay of 33 ns.
2. **74H00** series- the letter H standing for higher speed. It has a propagation delay of 6 ns but average power dissipation of 23 mW/gate.
3. **74S00**- the letter S representing Schottky. It has the highest speed because its average propagation delay is just 3 ns per gate. However, its average power dissipation is 23 mW/gate.
4. **74LS00** - it is the most recent variant of TTL family. It is called low-power Schottky TTL. It has an average propagation delay of 9.5 ns and an average power dissipation of 2mW.

**ECL Circuit**

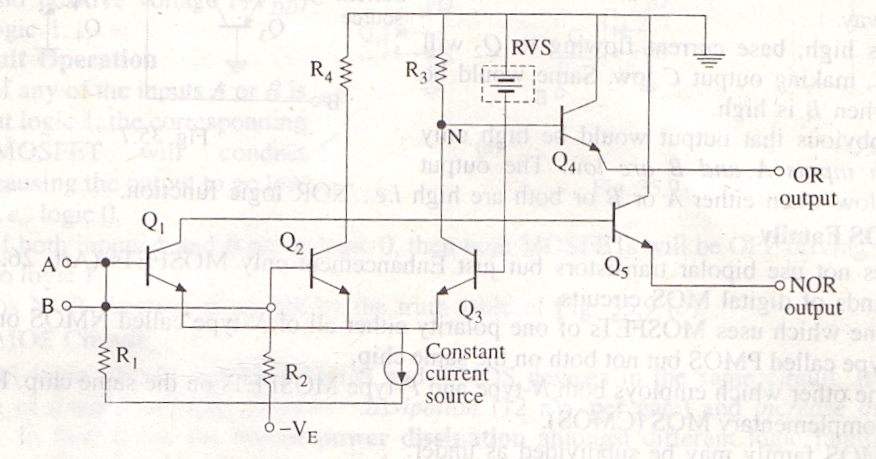
It has the highest speed of any of the currently-available logic circuits. It is primarily due to the fact that transistors never operate fully saturated or cut-off. That is why ECL is known as *non-saturated* logic. It has propagation delay time varying from 0.75 ns to 2 ns. However, power dissipation is increase since one transistor is always in the active region.

Another feature of ECL is that it provides two outputs which are always complement of each other (fig). It is so because the circuit operation is based on a differential amplifier.

This family is particularly suited to monolithic fabrication techniques because logic levels are function of resistor ratios.

**Circuit Operation**

The basic circuit shown in Fig. 5 is a combined OR/NOR circuit and is operated from a VEE= -5.2 V supply. A built-in constant-current source provides current to the emitters. Strictly speaking, logic 1 is represented by -0.9V (less negative) and logic 0 by - 1.75 V (more negative). Please note that it is a positive logic. Negative logic, the functions would be AND/NAND. A reference voltage of -1.3 V is applied to the base of Q3 from a built-in temperature-compensated reference voltage source (RVS).



**Figure 5.**

1. **When both inputs are logical 0 i.e., 1.75 V**

In this case, base potential of Q3 is less negative (or more positive) than the base potential of either Q1 or Q2. Hence, Q3 conducts whilst Q1 and Q2 do not. Only enough base current is drawn by Q3 from RVS so as to remain out of saturation. The collector current of Q3 develops a voltage of - 1.0 V across R3 which makes Q4 to conduct. Transistor Q4 gives an output voltage at the emitter of about -1.0-0.7 = -1.7 V which represents logic 0. Since collector potentials of Q1 and Q2 are nearly zero (because they are cut-off), the output voltage at the emitter of Q5 is 0-0.7 = -0.7 V which is a logic 1, Obviously, the two outputs are complements of each other.

1. **When either input A or B is at logical 1 i.e., -0.9V**

In that case, the associated transistor (either Q1 or Q2) is turned ON while Q3 is turned OFF. The collector potentials of Q1/Q2 and Q3 are opposite of the previous case. Hence, now Q5 output is at logical 1 and Q4 output is at logical 0.

**Typical characteristics of an ECL family are:**

1. Propagation delay time per gate of 1 us (meaning extremely fast speed),
2. Power dissipation of 30 mW
3. Fan-out of 50.
4. Fan-in of 5,
5. Noise immunity 0.4V.

There is another point worth noting about EL family. Since *all its logic levels are negative, it is not directly compatible with other logic series.* For interconnecting an ECL circuit and another circuit of a different family, a special level-shifting circuit has to he provided between the two. Such level-shifting circuits are available in IC packages and are usually referred to as **interface circuits.**

**I2 L Circuit**

It is the latest entry into the bipolar saturated logic field. It uses no biasing and loading resistors at all! Resistors require lot of power and space on an IC chip. Hence, their elimination results in higher density circuits operating at much reduce power. Because of its high speed and less power dissipation, it is used in large computers. Such circuits are also used where high packing density is of prime consideration as in digital wrist watches. I2L chips are capable of microwatt power dissipation yet can provide high currents when necessary to drive LED displays.

Another feature of I2L (integrated injection logic) is that it is easy to fabricate.

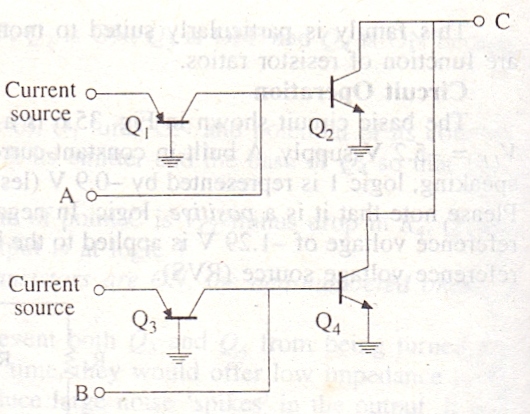
**Circuit Operation**

I2L NOR logic circuit is shown in Fig. 6. Here, transistors Q1 and Q2 act as current sources to the bases of Q3 and Q4 respectively.

If an input goes low, the current to the base of Q2 will be shorted to ground which will result in Q2 being turned OFF. The input B controls Q4 in similar way.

If A is high, base current flowing to Q2 will turn it ON, making output C low. Same would be the case when B is high.

It is obvious that output would be high only when both inputs A and B are low. The output would be low when either A or B or both are high i.e., NOR logic function.



**Figure 6.**

**MOS Family**:

It does not use bipolar transistors but just Enhancement -only MOSFETs. There are two kinds of digital MOS circuits.

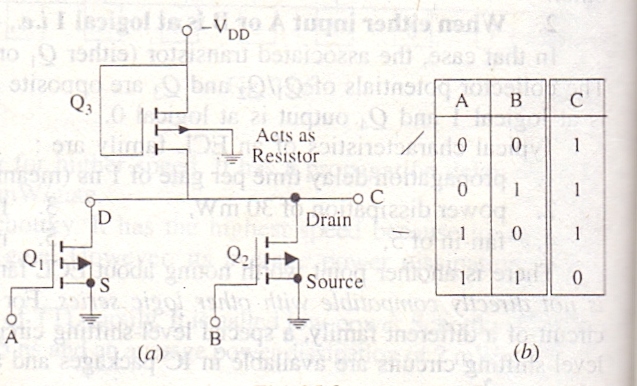
1. One which uses MOSFETs of one polarity either all of N-type called NMOS or all of P- type called PMOS but not both on the same chip,
2. The other which employs both N-type and P-type MOSFETs on the same chip. It is called complementary MOS (CMOS).

The MOS family may be subdivided as under:

Since a FET requires small area, it is possible to fabricate a large number of MOS circuits on a single small chip. Gating arrays with thousands of gates and flop-flops are manufactured in standard containers and are often used in IC memories and microprocessors.

**PMOS Circuit**

A PMOS NAND gate is shown is Fig. 7 (a). As seen, there is no resistors in the circuit. The gate consists of two E-only MOSFETs Q1 and Q2 as logic elements and the third one Q3 as load resistor. When-VDD (say-12V) is applied. MOSFETs will be turned ON and when 0 V is applied they would be turned OFF. Hence, with positive logic, 0 V would be 1 and -12 V would be 0 since 1 is assigned to the most positive voltage.



**Figure 7.**

**Circuit Operation**

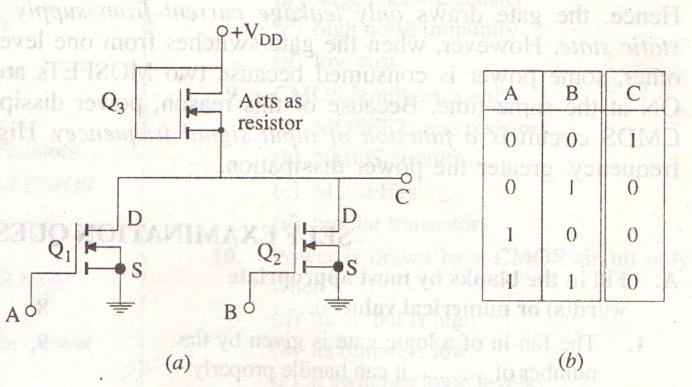
1. If any of the two inputs A or B is at logic 0 (i.e., -12 V), the concerned MOSFET would turn ON thereby offering a low resistance from drain to source thus causing the output to be nearly 0 V i.e., a logic 1.
2. The output can be at -12 V i.e., logic 0 only when both inputs A and B are at 0 V i.e., logic1.

This is the NAND function as shown by the truth table of Fig. 7(b)

Incidentally, the positive logic NAND gate of Fig (a) would be the negative logic NOR gate since the two are identical.

**NMOS Circuit**

In Fig. 8(a) is shown a two-input NOR gate circuit consisting of two MOSFETs Q1 and Q2 acting as logic elements and Q3 as a load resistor. For positive logic. 0 V will be logic 0 and positive voltage (+VDD) will be logic 1.



**Figure 8.**

**Circuit Operation**

1. If any of the inputs A or B is at logic1, the corresponding MOSFET will conduct causing the output to so low i.e., logic 0.
2. If both inputs A and B are at logic 0, then both MOSFETs will be OFF driving the output to logic1.

This is NOR function as shown by the truth table of Fig. 8(b).

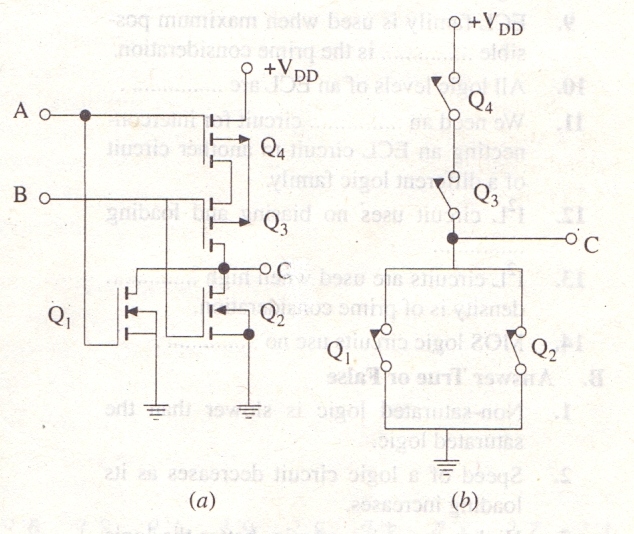
**CMOS Circuit**

CMOS logic circuits use both PMOS and NMOS devices in the same circuit. It gives the advantage of drastic decrease in power dissipation (12nW per fate) and increase in speed of operation. In fact, it has the lowest power dissipation amongst different logic families. It has very high packing density i.e., larger number of circuits can be placed on a single chip. As a result, it is extensively used in VLSI circuits such as one-chip computers and memory systems. The newest silicon-on-suphire MOS (SOS MOS) is 2 to 4 times faster than the standard CMOS. Hence, they are being widely used for everything from electronic watches and calculators to microprocessors.

Fig.9 (a) shows a CMOS NOR circuit which has two N-channel MOSFETs Q1 and Q2 and two P-channel MSFESTs Q3 and Q4. The two inputs A and B switch between +VDD (logic1) and ground (logic 0).

**Circuit Operation:**

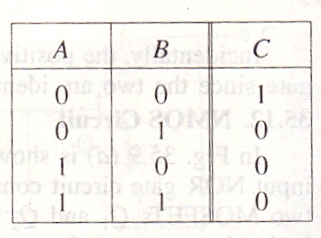
1. Let A= B = logic 1 i.e., have positive voltage. In that case, Q1 and Q2 are ON (closed switches) but Q3 and Q4 are OFF and act as open switches as shown in Fig. 9(b), hence, output C is logic 0.
2. If either A or B is at logic 1, then the associated N-channel MOSFETs (Q1 or Q2) is turned ON but the associated P-channel MOSFET (Q3 or Q4) is turned OFF. Since either Q3 or Q4 would be OFF [fig. 9(b)] output c would be at logic 0.

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**Figure 9.**

1. When both A and B are at logic 0, Q3 and Q4 would be ON but 1 and Q2 would be OFF- just the opposite of that in Fig. 9(b). Hence, output C would be at logic 1 (remember, voltage across an open equals the supply voltage.

The above logic represents a NOR function as shown in the truth table of Fig. 10. It would be observed from fig. that in each combination of A and B, there is at least one open switch between +VDD and Ground. Hence, the gate draws *only leakage current from supply for any static state*. However, when the gate switches from one level to another, same power is consumed because two MOSFETs are partly ON at the same time. Because of this reason, power dissipated by CMOS circuit is a function of input signal frequency. Higher the frequency, greater the power dissipation.



**Figure 10.**