**HOME ASSIGNMENT**

**VLSI Design (VI – SEMESTER)**

**(2017-2018)**

**Electrical and Electronics Engineering**

(1) Draw the stick diagrams with colour pen/pencil/sticks of two input NAND gate and NOR gate, RS-Lach and clocked JK FF.

(2) What is latch up problem in an N well and P-well CMOSFET? Explain how it affects threshold voltage.

(3) Write down the λ based design rules with suitable the diagrams.

(4) Describe VLSI design problems along with its design methodology Y-chart. Discuss how different domains are transferred mapped to another domain.

(5) What are the ways of heat transfer from an IC? Explain them briefly and also describe the packaging of an integrated circuit with some idea of its design economics.

(6) Explain FPGA with a mention of its various types.



(7) Design the complex logic circuits of expression through CMOS logic design and also calculate its logical effort.

(8) Design a full adder circuit through CMOS realization by assuming its inputs and carry.

(9) Design RS-latch with clock through NOR gates and NAND gates with CMOS realization.

(10) Explain CLB and 4 and 3-input look up table with suitable diagram.

(11) Define (i) critical path (ii) arrival time (iii) required time and (iv) slack.

(12) Implement the following Boolean function using PLA:



(13) Calculate logical effort and parasitic delay of a three input NAND gate. Also estimate the propagation delay of NMOS inverter if its

(i) ZPU / ZPD = 4 : 1, τ = 0.4 ns. (ii) ZPU / ZPD = 8 : 1, τ = 0.5 ns. Define different delays.

(14) Write a short note on (i) FPGA (ii) ASIC (iii) Stick diagrams (iv) ROM (v) PAL

(15) Write a short note on

(i) the BIST technique (ii) Ad hoc techniques (iii) Scan technique (iv) BILBO