HOME ASSIGNMENT-2

Q1. Consider a 6mm long 0.32 µm wide metal2 wire in 65 nm process . The sheet resistance is 0.05 Ω / square and capacitance is 0.02 fF/µm. construct a 3-segment π –model for the wire. Also calculate dynamic power if activity factor is 0.8,operating votage is 1V, switching capacitance is 10fF with clock frequency of 3MHz. Sketch the interconnect models

Q2.Explain the fabrication process steps of CMOS Inverter and its mask set with suitable diagrams. What is difference between SRAM and DRAM

Q3. Write down the λ- based design rules of the MOSFET circuits. Draw stick diagram of two input NAND gate with clear legends. Where is activity factor used?

Q4.Explain and find the linear delay Model, logical Effort and parasitic delay of an inverter, two input NAND gate and NOR gates. Define domino logic circuit

Q5. The circuit in the following fig. Q.5. has non uniform branching, reconvergent fan-out and a wire load in the middle of the path, all of which stymie back of the envelope application of Logical effort. the wire load is given in the same units as the gate capacitances.Assume the inputs arrive at Time 0.write an expression for the arrival time of the output as a function of the gate drives. Determine the sizes to achieve minimum delay. Define propagation delay and contamination delay

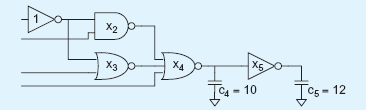


Fig.Q.5

Q6.Descrbe the ways to reduce the power in micro architecture and power management modes. Define pitch and aspect ratio on the interconnect  
Q7. Differentiate between pass transistor and transmission gate .Explain in detail the energy delay optimization of MOSFET.

Q8. Write about SRAM with read and write - operation and Fault Types and their Models with examples.

Q9.Classify the levels of integration of chips .Explain the synchronous dynamic circuit techniques (a)Multistage pass transistor logic driven by two non overlapping clocks (b) Three stages of a depletion load nMOS dynamic SR circuit driven by two phase clocking

Q10. Why are the CMOS processes widely adopted? Differentiate between ratioed and non -ratioed circuits with pre-charge and evaluate logic circuits. Also briefly describe adiabatic logic circuit.

Q11. Who developed IC and when? Briefly describe all the interconnect impacts like delay,crosstalk,energy andinductivee effects.

Why has the BIST approach been integrated on the chip? Explain it.

Q12.What are potential failure modes under the reliability factor of interconnects? Q13.What are the AD HOC testable Design Techniques? Explain briefly each of them ?

Q14. Analyze propagation delay and contamination delay for two input NAND and three input NOR –gates for every switching combination such as for 00,01,10 and 11 for NAND-2 gate and 000,001,010,011,100,101,110 ,111 for NOR-3 gate.

Q15. Discuss all the steps of masking and fabricating two input NAND gate with its stick diagram.