1a) Define VLSI, MSI, and SSI.

The first integrated circuits contained only a few transistors and so were called “Small-Scale Integration (SSI). SSI was followed by introduction of the devices which contained hundreds of transistors on each chip.Medium-Scale Integration (MSI). Very Large Scale Integration (VLSI) where hundreds of thousands of transistors were used.

1b) Name any two basic CAD tools and explain.

Cadence, VHDL,Verilog,PsPICE,HSPICE,TCADS etc.

1c) Define Noise margin and propagation delay.

Noise Margin : Ability of the gate to tolerate fluctuations of the voltage levels.

NMH ≡ VOH - VIH noise margin high NML ≡ VIL - VOL noise margin low

Propagation delay : symbolized t_{pd}, is the time required for a digital signal to travel from the input of a logic gate to the output. It is measured in microseconds (µs), nanoseconds (ns).

1d) What do you meant by threshold voltage of MOS transistor?

The MOSFET $V_{GS(th)}$ or gate threshold voltage is the voltage between the gate and source that is needed to turn on the MOSFET. In other words, if V_{GS} is at least as high as the threshold voltage, the MOSFET turns on.

1e) Distinguish between SRAM and DRAM.

SRAM and DRAM are the modes of integrated-circuit RAM where SRAM uses transistors and latches in construction while DRAM uses capacitors and transistors. These can be differentiated in many ways, such as SRAM is comparatively faster than DRAM; hence SRAM is used for cache memory while DRAM is used for main memory.

2a) Analyze the Characteristics of CMOS Inverter With neat Sketch.

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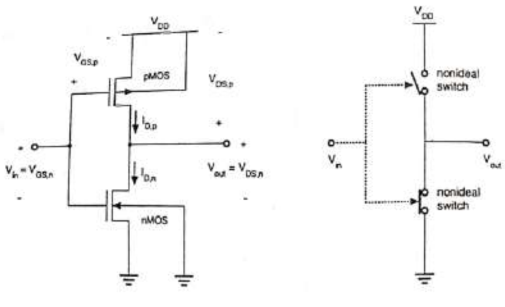
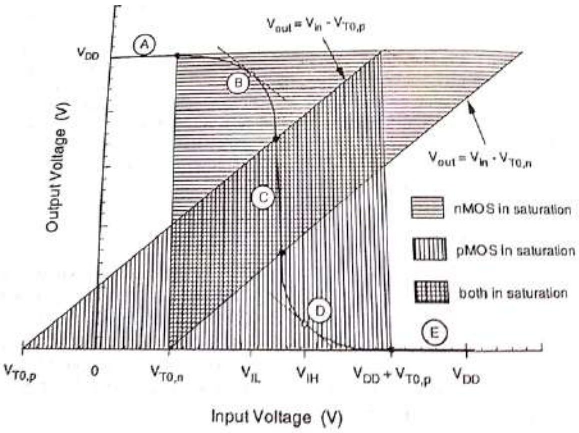


(a) (a) CMOS inverter circuit.

(b) (b) Simplified view of the CMOS

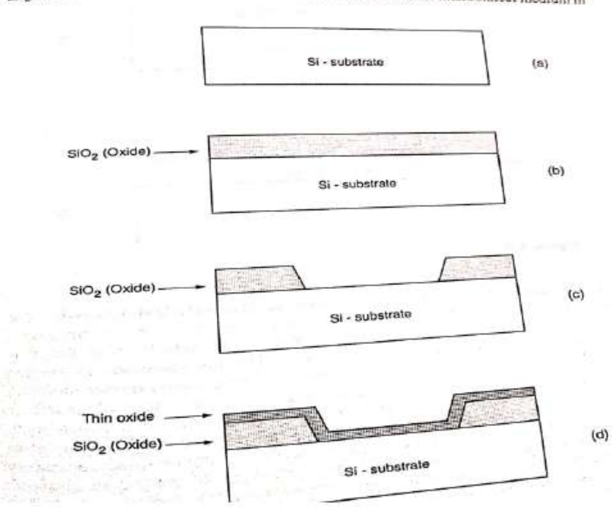


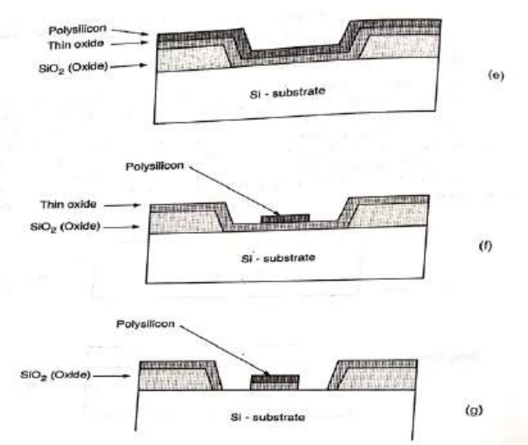
In this general configuration, the input signal is always applied to the gate of the driver transistor, and the operation of the inverter is controlled primarily by switching the driver. Now, we will turn our attention to a radically different inverter structure, which consists of an enhancement-type nMOS transistor and an enhancement-type pMOS transistor, operating in complementary mode ( ). This configuration is called Complementary MOS (CMOS). The circuit topology is complementary push-pull in the sense that for high input, the nMOS transistor drives (pulls down) the output node while the pMOS transistor acts as the load, and for low input the pMOS transistor drives (pulls up) the output node while the nMOS transistor acts as the load. Consequently, both devices contribute equally to the circuit operation characteristics.

The CMOS inverter has two important advantages over the other inverter configurations. The first and perhaps the most important advantage is that the steady-state power dissipation of the CMOS inverter circuit is virtually negligible, except for small power dissipation due to leakage currents. However, as mentioned earlier, the trend of increasing subthreshold leakage currents in deep sub-micron technologies causes great design challenges. In all other inverter structures examined so far, a nonzero steady-state current is drawn from the power source when the driver transistor is turned on, which results in a significant DC power consumption.

2 b)

The process starts with the oxidation of the silicon substrate in which a relatively thick silicon dioxide layer, also called field oxide, is created on the surface. Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created. Following this step, the surface is covered with a thin, high-quality oxide layer, which will eventually form the gate oxide of the MOS transistor. On top of the thin oxide layer, a layer of polysilicon (polycrystalline silicon) is deposited. Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in





silicon integrated circuits. Undoped polysilicon has relatively high resistivity. The resistivity of polysilicon can be reduced, however, by doping it with impurity atoms.

After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates. The thin gate oxide not covered by polysilicon is also etched away, which exposes the bare silicon surface on which the source and drain junctions are to be formed. The entire silicon surface is then doped with a high concentration of impurities, either through diffusion or ion implantation (in this case with donor atoms to produce n-type doping). shows that the doping penetrates the exposed areas on the silicon surface, ultimately creating two n-type regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity. Note that the polysilicon gate, which is patterned *before* doping, actually defines the precise location of the channel region and, hence, the location of the source and the drain regions.

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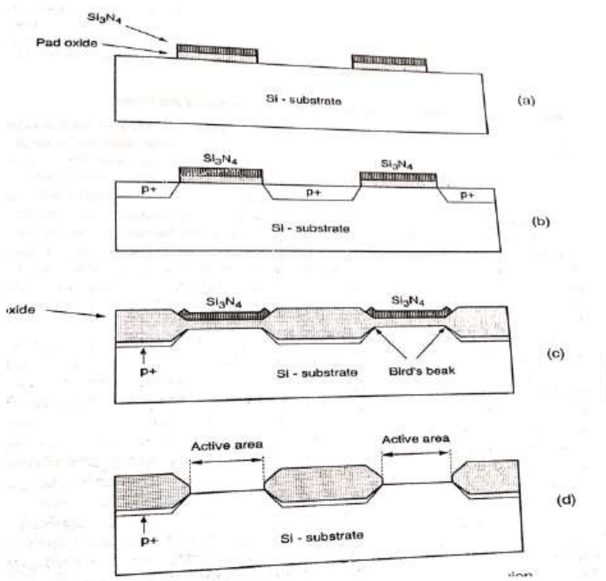
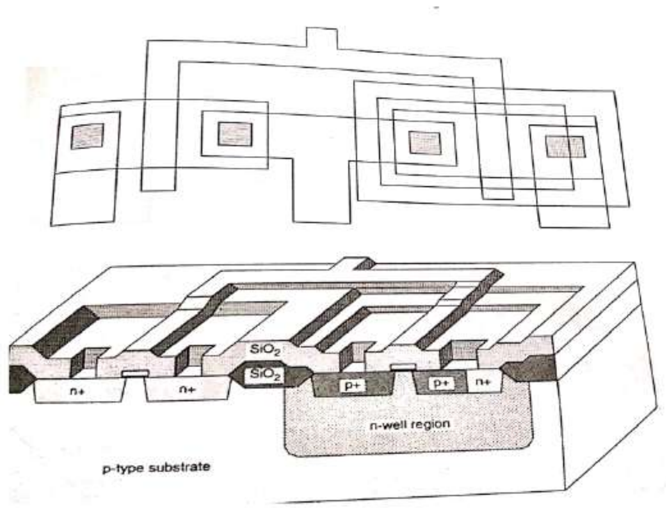
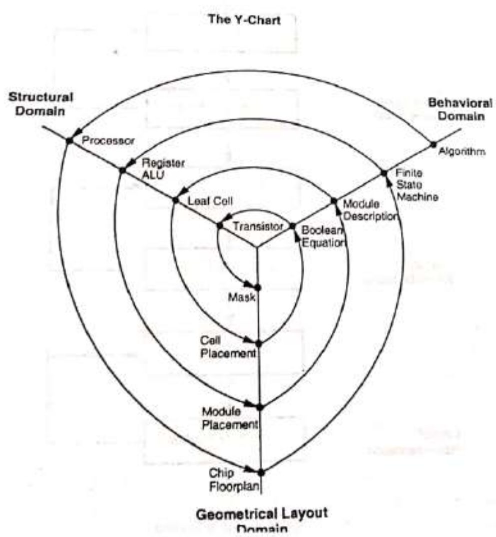




4a)

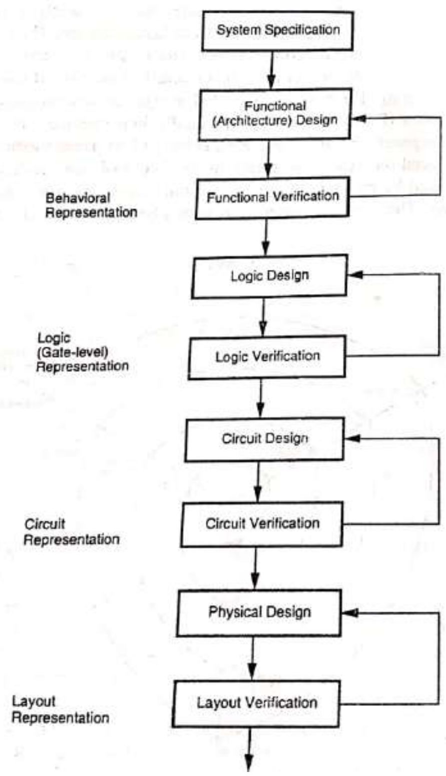
The design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirements. Initial design is developed and tested against the requirements. When requirements are not met, the design has to be improved. If such improvement is either not possible or too costly, then a revision of requirements and an impact analysis must be considered. The Y-chart (first introduced by D. Gajski) shown in Fig. 1.20 illustrates a simplified design flow for most logic chips, using design activities on three different axes (domains) which resemble the letter "Y." In reality, there exist many feedback loops that are not shown for simplicity.

The Y-chart consists of three domains of representation, namely (i) behavioral domain, (ii) structural domain, and (iii) geometrical layout domain. The design flow starts from the *algorithm* that describes the behavior of the target chip. The corresponding *architecture of the processor* is first defined. It is mapped onto the chip surface by *floorplanning*. The next design evolution in the behavioral domain defines *finite state machines* (FSMs) which are structurally implemented with *functional modules* such as registers and arithmetic logic units (ALUs). These modules are then geometrically placed onto the chip surface using CAD tools for automatic *module placement* followed by routing, with a goal of minimizing the interconnects' area and signal delays. The third evolution starts with a behavioral *module description*.



Individual modules are then implemented with *leaf cells*. At this stage the chip is described in terms of logic gates (leaf cells), which can be placed and interconnected by using a *cell placement and routing* program. The last evolution involves a detailed *Boolean description* of leaf cells followed by a transistor level implementation of leaf cells and *mask generation*. In the standard-cell based design style, leaf cells are pre-designed (at the transistor level) and stored in a library for logic implementation, effectively eliminating the need for the transistor level design.

Figure 1.21 provides a more simplified view of the VLSI design flow, taking into account the various representations, or abstractions of design: behavioral, logic, circuit



4 b)

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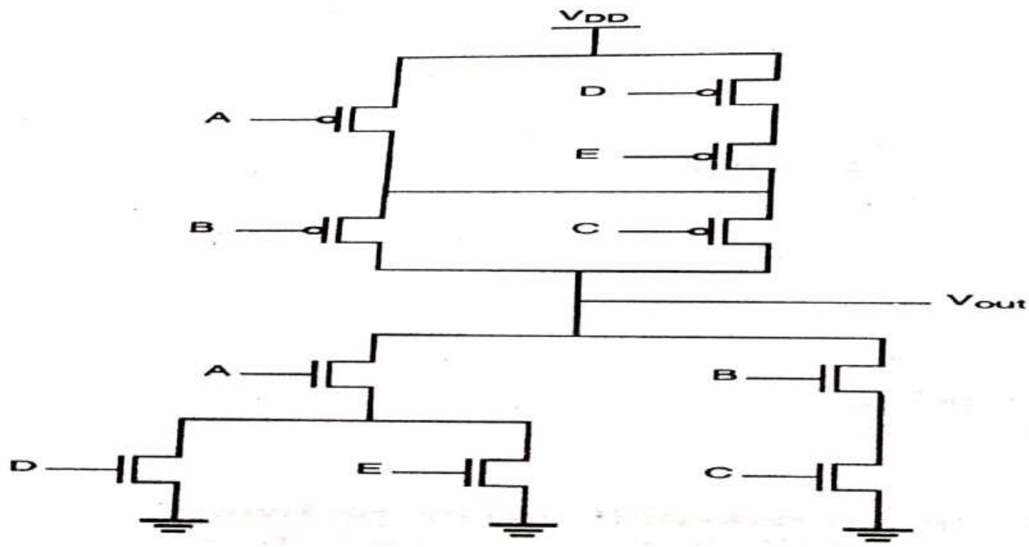
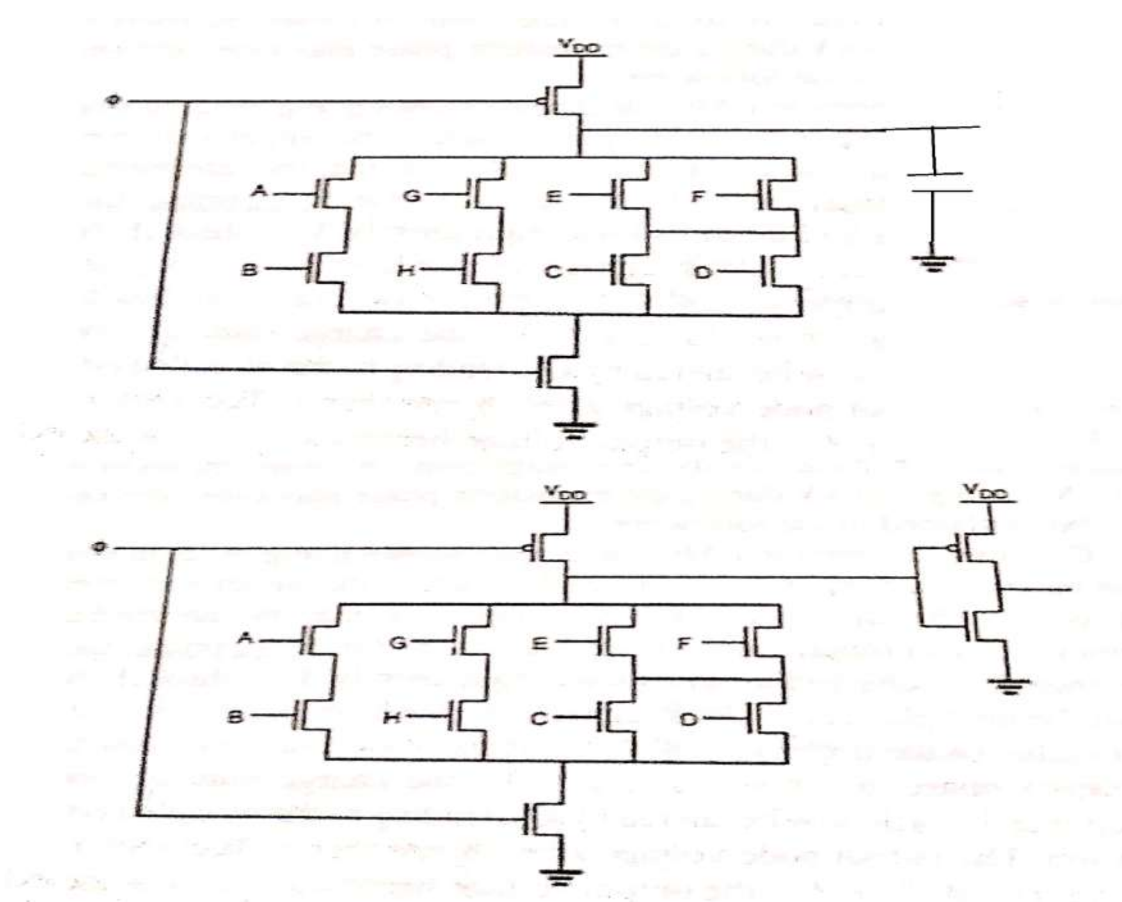
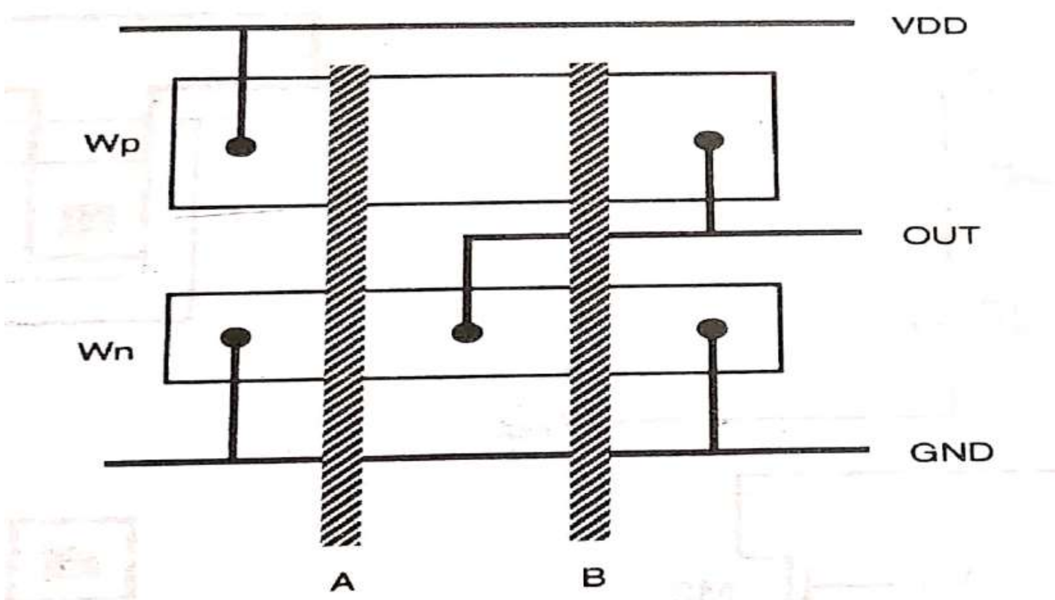


5a)



5b)


VDD
Wp
OUT
Wn
GND
A
B