Solution Subject : Electronics Engineering Subject Code : KOE038

B.Tech. 3rd SEMESTER

SECOND SESSIONAL EXAMINATION, ODD SEMESTER, (2019-2020)

Branch : Computer Science & Engineering, Electrical Engineering

Time –1hr 30 min **Maximum Marks – 30**

SECTION - A

Q-1) Attempt ALL parts- **(5*1 = 05)**

a) What is PIV for Center tap and Bridge rectifier?
ANS : Center tap = **$2V_m$ and** Bridge rectifier = **V_m**

b) What is meant by a clipping circuit?
ANS : A wave shaping circuit which controls the shape of the output wave form by removing of unwanted portion of input wave is known as clipping circuit.

c) Compare LED and LCD.
ANS : Comparison of LED and LCD.

LEDs	LCDs
1. More power is required	1. Less power is required.
2. Fastest displays.	2. Slowest display
3. More life.	3. Less life

d) Write relation between α and β.

$$\alpha = \frac{\beta}{1+\beta} \qquad \beta = \frac{\alpha}{1-\alpha}$$

ANS :

e) Define pinch-off voltage.
Ans : Pinch off voltage: Pinch off voltage is the drain to source voltage after which the drain to source current becomes almost constant.

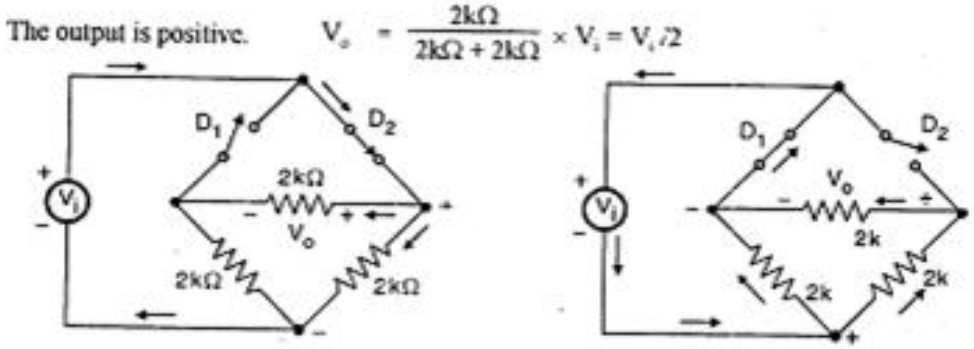
SECTION - B

Q 2) Attempt any TWO parts from this section. **(2*5 = 10)**

a. Determine the voltage Vo for the given figure**.**

ANS : Assume D1 and D2 to be ideal diodes.

Operation in the positive half cycle: fig 2b shows the equivalent circuit in the positive half cycle



2b Equivalent circuit in the positive half cycle 2c Equivalent circuit in the negative half cycle

Operation in the negative half cycle: fig 2c shows the equivalent circuit in the positive half cycle.

$$\therefore V_o = \frac{2k\Omega}{2k\Omega + 2k\Omega} \times V_i = V_i/2$$ and the output is positive.

b. Find the range of I_L and R_L for the circuit (figure 2 B) if the output voltage is to be maintaining constant at 10 V.

ANS :

$$\text{Supply current, } I_S = \frac{V_{in} - V_L}{R} = \frac{50 - 10}{1{,}000} = 40 \text{ mA}$$

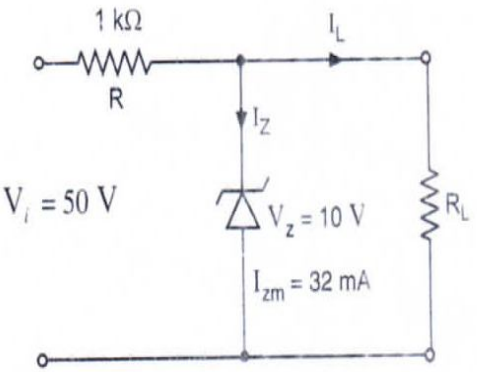


Figure Q 2 B

Load current I_L will be maximum when zener current $I_Z = 0$ A

So $I_{L\,max} = I_S - I_{Z\,min} = 40$ mA **Ans.**

Corresponding load resistance will be minimum and so

$$R_{L\,min} = \frac{V_L}{I_{L\,max}} = \frac{V_Z}{I_{L\,max}} = \frac{10}{40 \times 10^{-3}} = 250\ \Omega \text{ Ans.}$$

Load current I_L will be minimum when zener current I_Z is maximum *i.e.*, 32 mA

So, $I_{L\,min} = 40 - 32 = 8$ mA **Ans.**

Corresponding load resistance will be maximum, so

$$R_{L\,max} = \frac{10}{8 \times 10^{-3}} = 1{,}250\ \Omega \text{ Ans.}$$

Thus, I_L ranges from 8 mA to 40 mA and R_L ranges from 250 Ω to 1,250 Ω } **Ans.**

c. Determine I_C, V_E, V_B , V_C and I_B for the following circuit in figure 2 C.

ANS :

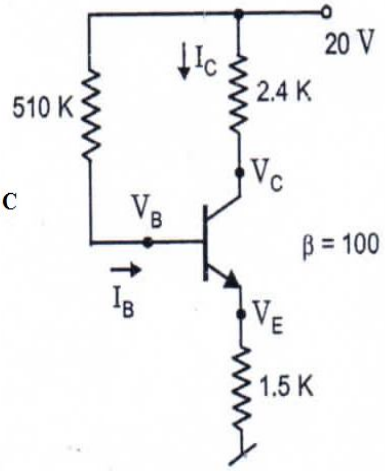


Figure Q 2 C

For given emitter bias CE amplifier,

$R_B = 510$ kΩ

$R_C = 2.4$ kΩ

$R_E = 1.5$ kΩ

$V_{CC} = 20$ V

and $\beta = 100$

Applying KVL for the input loop,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$$

$$\text{or } I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} = \frac{20 - 0.7}{510 \times 10^3 + 101 \times 1.5 \times 10^3} = \frac{19.3}{661.5 \times 10^3} = 0.0292 \text{ mA Ans.}$$

So collector current, $I_C = \beta I_B = 100 \times 0.0292 = 2.92$ mA **Ans.**

Collector voltage, $V_C = V_{CC} - I_C R_C = 20 - 2.92 \times 10^{-3} \times 2.4 \times 10^3 = 13$ V **Ans.**

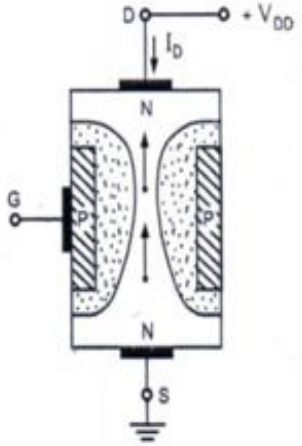
Emitter voltage, $V_E = I_E R_E = (\beta + 1) I_B R_E = 101 \times 0.0292 \times 10^{-3} \times 1.5 \times 10^3 = 4.42$ V **Ans.**

Base voltage, $V_B = V_{CC} - I_B R_B = 20 - 0.0292 \times 10^{-3} \times 510 \times 10^3 = 5.12$ V **Ans.**

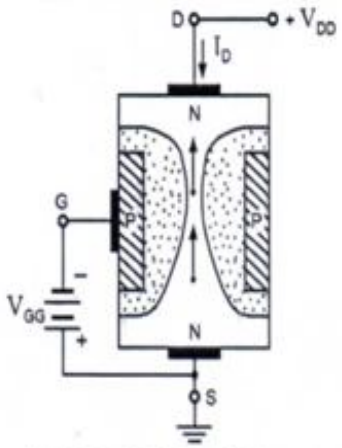
d. Explain the working of n channel JFET.

ANS :

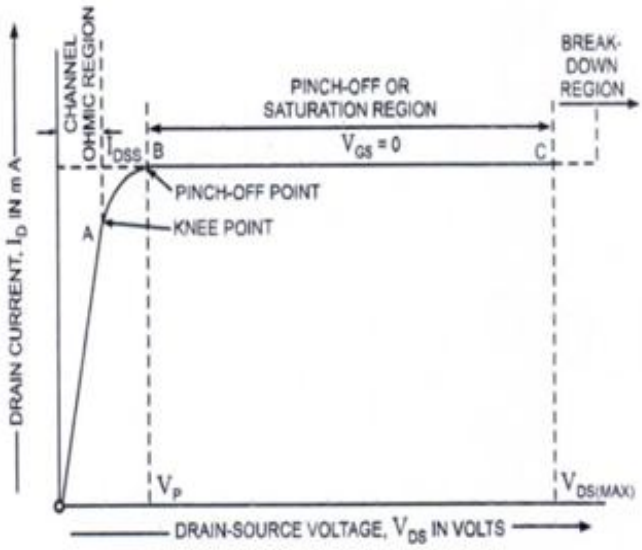
(*i*) When neither any bias is applied to the gate (*i.e.*, when $V_{GS} = 0$) nor any voltage to the drain w.r.t. source (*i.e.*, when $V_{DS} = 0$), the depletion regions around the P-N junctions are of equal thickness and symmetrical.



(a) JFET With No Bias Voltage



(b) JFET With Small Negative Gate Source Bias



JFET Drain Characteristic With Shorted Gate

The amount of reverse bias is not the same throughout the length of the P-N junction. When the drain current flows through the channel, there is a voltage drop along its length. The result is that the reverse bias at the drain end is more than that at the source end making the width of depletion layer more at the drain end than that at the source end. Thus the channel becomes narrower at the drain end in comparison to that at source end,

The reverse bias is more at the drain end than that at the source end of the channel, so with the increase in V_{DS}, the conducting portion of the channel begins to constrict more at the drain end. Eventually a voltage V_{DS} is reached at which the channel is *pinched off*. The drain current I_D no longer increases with the increase in V_{DS}. It approaches a constant saturation value. The value of voltage V_{DS} at which the channel is pinched off (*i.e.*, all the free charges from the channel get removed), is called the *pinch-off voltage* V_p.

SECTION - C

3. Attempt any ONE part of the following : (1*5 = 5)

a) Explain the working and characteristic of Tunnel diode.

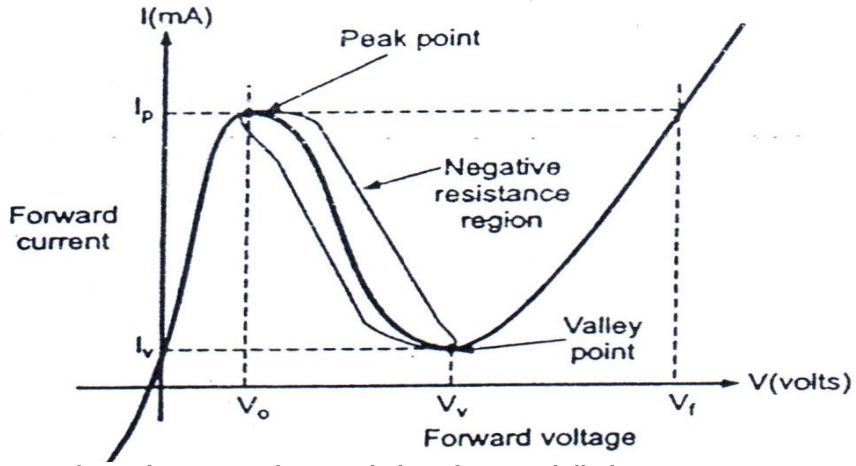
ANS : TUNNEL DIODE : A normal *p-n* junction has an impurity concentration of about 1 part in 10^8. This much amount of doping has the depletion layer width of about 5 microns. the diodes in which the concentrate on of imparity atoms is greatly increased upto 1 part in 10^3, to get completely changed characteristics, are called as *Tunnel diodes*. Theses diodes are first introduced by Leo Esaki in 1958.

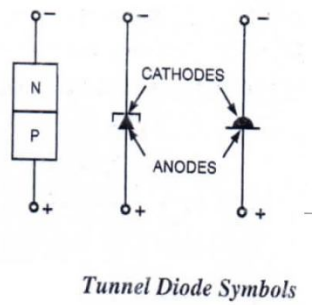
Due to the heavy doping the depletion region gets reduced considerably, of the order of 10^{-6} cm i.e. about 1/100 the width of depletion region in normal *p-n junction* diode.

Due to the thin depletion region, an electron penetrates through the barrier. This is called as tunneling and hence such high impurity density p-n junction devices are called as *tunnel diodes*.

Many carriers in tunnel diodes penetrate the barrier at velocities far more than the velocities available in the conventional diodes, at low forward bias voltages. Due to such effect, it shows a negative resistance region in its volt-ampere characteristics. This negative resistance region is the most important feature of a tunnel diode.

Characteristics of tunnel diode : Figure shows the volt-ampere characteristics of a tunnel diode.



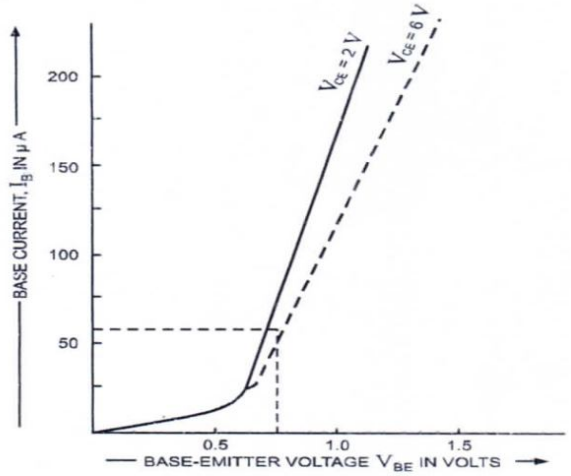


Tunnel Diode Symbols

Fig: volt-ampere characteristics of a tunnel diode.

b) Explain the input and output characteristics of BJT in the CE configuration.

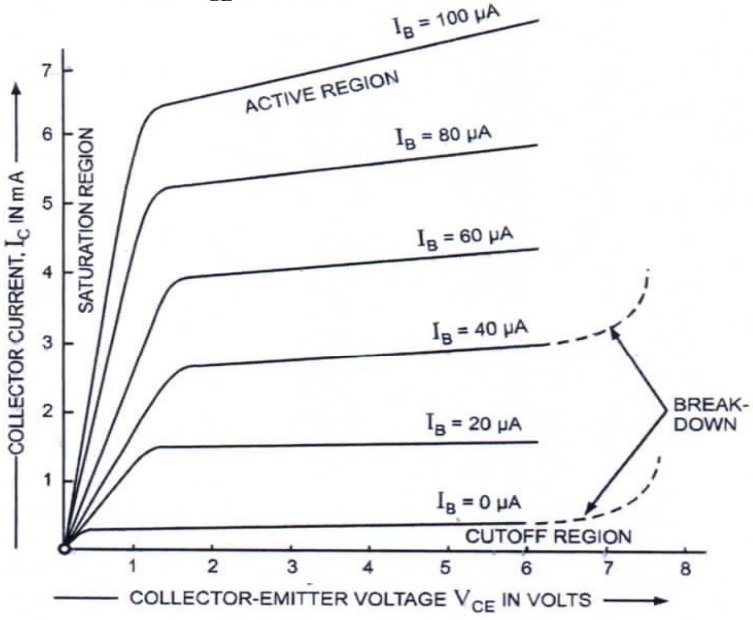
Ans :



Input Characteristics For Common Emitter NPN Transistor

Input Characteristics. The curve drawn between base current I_B and base-emitter voltage V_{BE} for a given value of collector-emitter voltage V_{CE} is known as the *input characteristic.*

Output Characteristics. Output characteristic for a common emitter transistor is the curve drawn between collector current I_C and collector-emitter voltage V_{CE} for a given value of base current I_B.



Output Characteristics For Common Emitter NPN Transistor

4. Attempt any ONE part of the following : **(1*5 = 5)**

a) For a voltage divider biasing circuit (figure 4 A), Calculate I_B, I_C, and V_{CE}.

Answer

Applying Thevenin's theorem to given potential divider network, we have

Thevenin's resistance, $R_{Th} = R_1 \| R_2$

$$= \frac{R_1 \times R_2}{R_1 + R_2} = \frac{47 \times 5.6}{47 + 5.6}\ k\Omega = 5\ k\Omega$$

Thevenin's voltage, $V_{Th} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{5.6}{47 + 5.6} \times 20 = 2.13\ V$

The circuit will be redrawn as shown in Figure 4 B

Applying KVL in input loop, we have

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E = I_B R_{Th} + V_{BE} + (1+\beta) I_B R_E$$

$$\text{or } I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} = \frac{2.13 - 0.7}{5 \times 10^3 + (150 + 1) \times 1 \times 10^3}$$

$$= 9.2\ \mu A \quad \textbf{Ans.}$$

Collector current, $I_C = \beta I_B = 150 \times 9.2 \times 10^{-6} = 1.375\ mA$ **Ans.**

Emitter current, $I_E = I_C + I_B = 1.375 + 0.0092 = 1.384\ mA$

Emitter voltage, $V_E = I_E R_E = 1.384 \times 10^{-3} \times 1 \times 10^3 = 1.384\ V$ **Ans.**

Base voltage, $V_B = V_{BE} + V_E = 0.7 + 1.384 = 2.084\ V$ **Ans.**

Applying KVL in output loop

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 20 - 1.375 \times 10^{-3} \times 2.2 \times 10^3 - 1.384 = 15.6\ V \quad \textbf{Ans.}$$

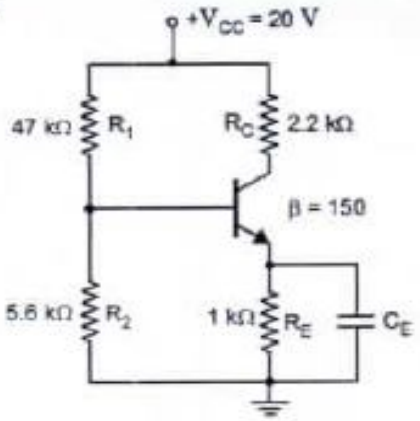
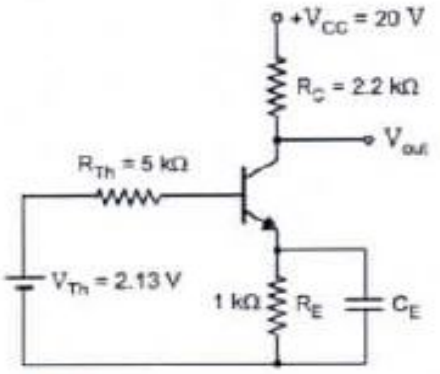
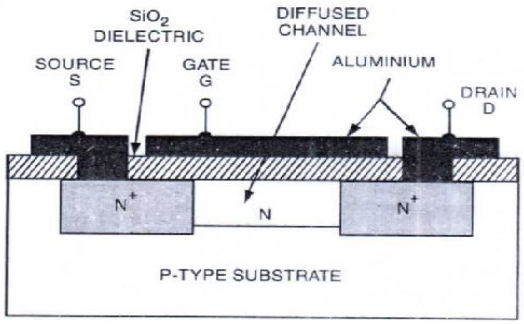


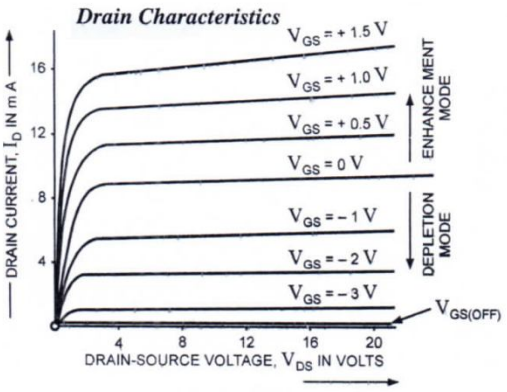
Figure 4 A

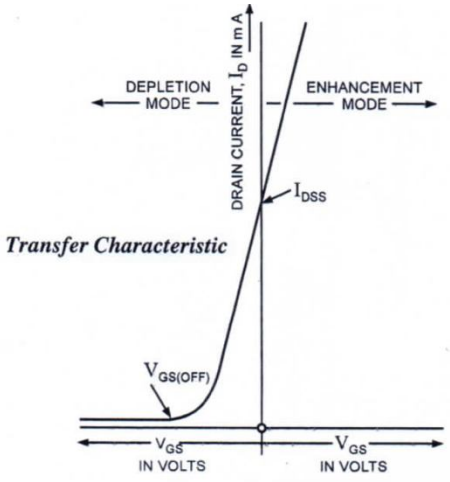


b) Draw the construction of N channel D MOSFET. Draw Drain and Transfer characteristic.



Answer :

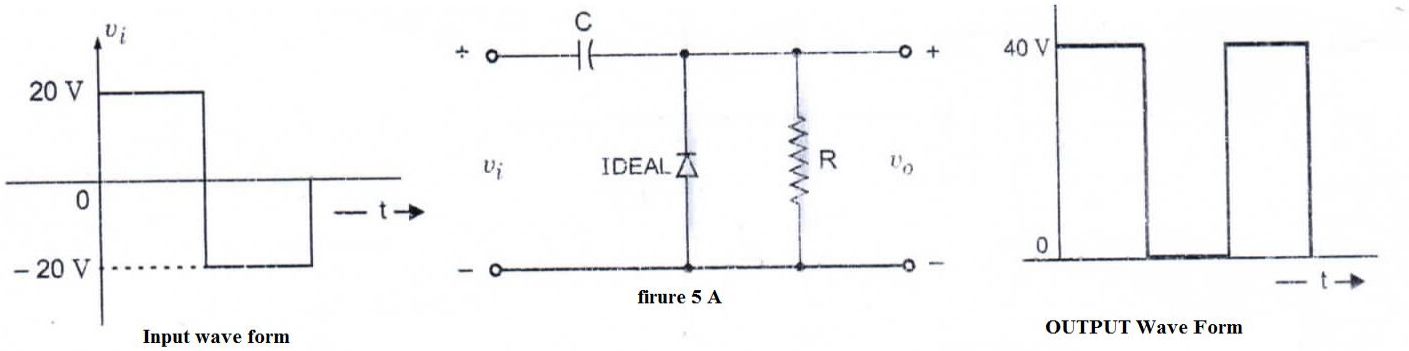




5. Attempt any ONE part of the following : **(1*5 = 5)**

a) Sketch Vo for the given Vi in circuit (figure 5 A).

ANS :



Input wave form

firure 5 A

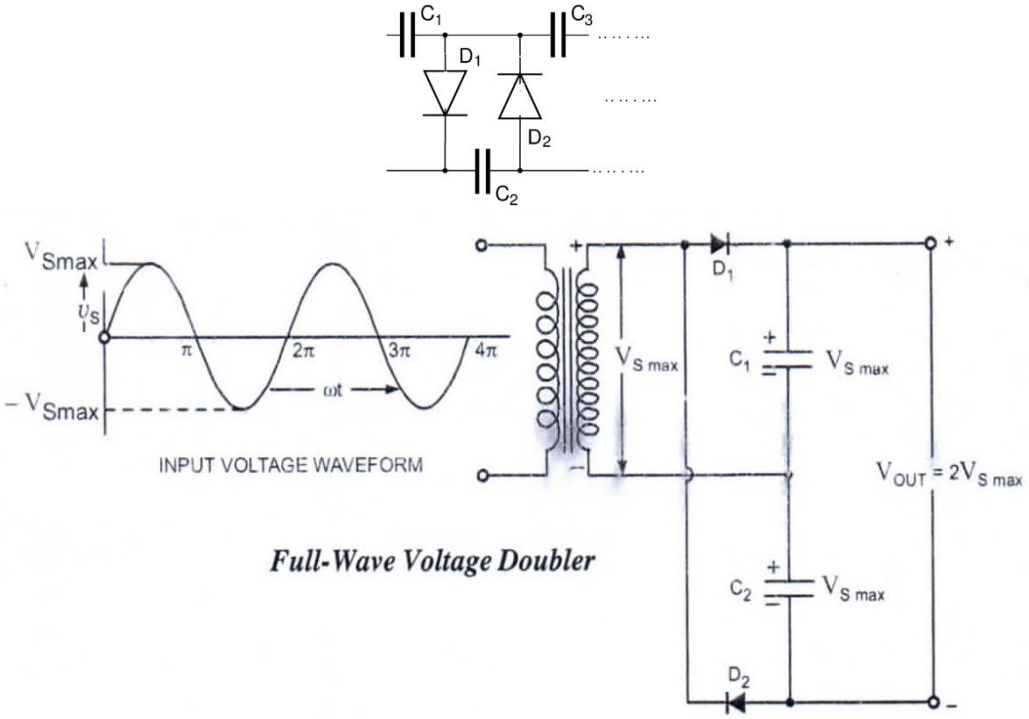
OUTPUT Wave Form

Given circuit is of positive clamper. In positive half cycle, capacitor will shift the voltage to positive direction and output voltage will be $2 \times V_{in} = 40$ V.

During negative half cycle, diode will be forward biased and there is no voltage drop across diode (diode being ideal) and therefore output voltage will be zero. Output waveform is shown in Fig.

b) What is voltage multiplier. Draw and explain the voltage Doubler circuit.

Answer : A voltage multiplier is a circuit that converts lower voltage to a higher voltage, It is a a network of capacitors and diodes.



Full-Wave Voltage Doubler

Full-Wave Voltage Doubler

The circuit diagram for a full-wave voltage doubler is given in Fig. During the positive cycle of the ac input voltage, diode D_1 gets forward biased and so conducts charging the capacitor C_1 to a peak voltage $V_{S\,max}$ with polarity indicated in the figure, while diode D_2 is reverse biased and does not conduct. During the negative half cycle, diode D_2 being forward biased conducts and charges the capacitor C_2 with polarity shown in the figure while diode D_1 does not conduct. With no load connected to the output terminals, the output voltage will be equal to sum of voltages across capacitors C_1 and C_2 *i.e.*, $V_{C_1} + V_{C_2}$ or $(V_{S\,max} + V_{S\,max})$ or $2\,V_{S\,max}$. When the load is connected to the output terminals, the output voltage V_L will be somewhat less than $2\,V_{S\,max}$. The input voltage and output voltage waveforms are also shown in Fig.