→ LONG ANSWER TYPE QUESTION

Ans. 1 Addressing Modes of 8051 Microcontroller are

(i) Immediate Addressing :

- In this addressing mode source operand is a constant rather than a variable.
- Sign "#" indicates it is a immediate addressing mode.
- For eg. - MOV A, #52H

(ii) Register Addressing :

- In this mode, the data to be operated is within the registers.
- 8051 can access eight "working registers" (R0 - R7).
- For eg. - MOV A, R3 : Copies content from R3 to A

(iii) Direct Addressing :

- Direct Addressing Mode can access any on-chip variable or hardware register, i.e., on-chip RAM and special fn reg.

- For eg.- • MOV R0, 40H
  • MOV 56H, A

- These reg. (R0-R7) can be accessed in two ways.
  For eg.- MOV A, 4
  Similar to MOV A, R4.

(iv) Register Indirect Addressing :

- In this mode, a register is used as a pointer to point the data.
- Data inside the CPU can be pointed by registers R0 and R1 only.
- The instruction with indirect addressing uses the "@" sign.
- For eg.- MOV A, @R0.
  MOV @R1, B.

(v) Relative Addressing :

- The JMP (Jump) and CALL instructions in 8051 are used in this mode.
- In this, a new program address is not directed specified. It is specified as difference in bytes. of new address from the

address in program counter called offset.

(vi) Absolute Addressing :

- This mode is similar to that of relative addressing except the offset length.
- The offset is 11-bit instead of 8-bit in case of relative addressing.
- AJMP and ACALL uses addressing mode of absolute.

(vii) Long Addressing :

- In this, the new address of JMP or CALL instruction (LJMP or LCALL) is specified as entire new 16-bit addresses.
- A jump or call can be made to location within 64-Kbyte code memory space.

(viii) Indexed Addressing :

- Only program memory can be accessed in this mode.
- Either the DPTR or PC can be used as an index register.

- For eg. – • MOVC A, @A + DPTR
  → Copies the content of memory location pointed by sum of A and DPTR into A.
  • MOV A, @A + PC

(ix) Inherent Addressing :

- Inherent in instruction, these refers to a specific register such as accumulator or DPTR.

- For eg. – SWAP A : Swap nibbles within A.

(x) Bit - Inherent Addressing :

- The address of the flag which contains the operand, is implied in the opcode of the instruction.

- For eg. – CLR C.

(xi) Bit - Direct Addressing :

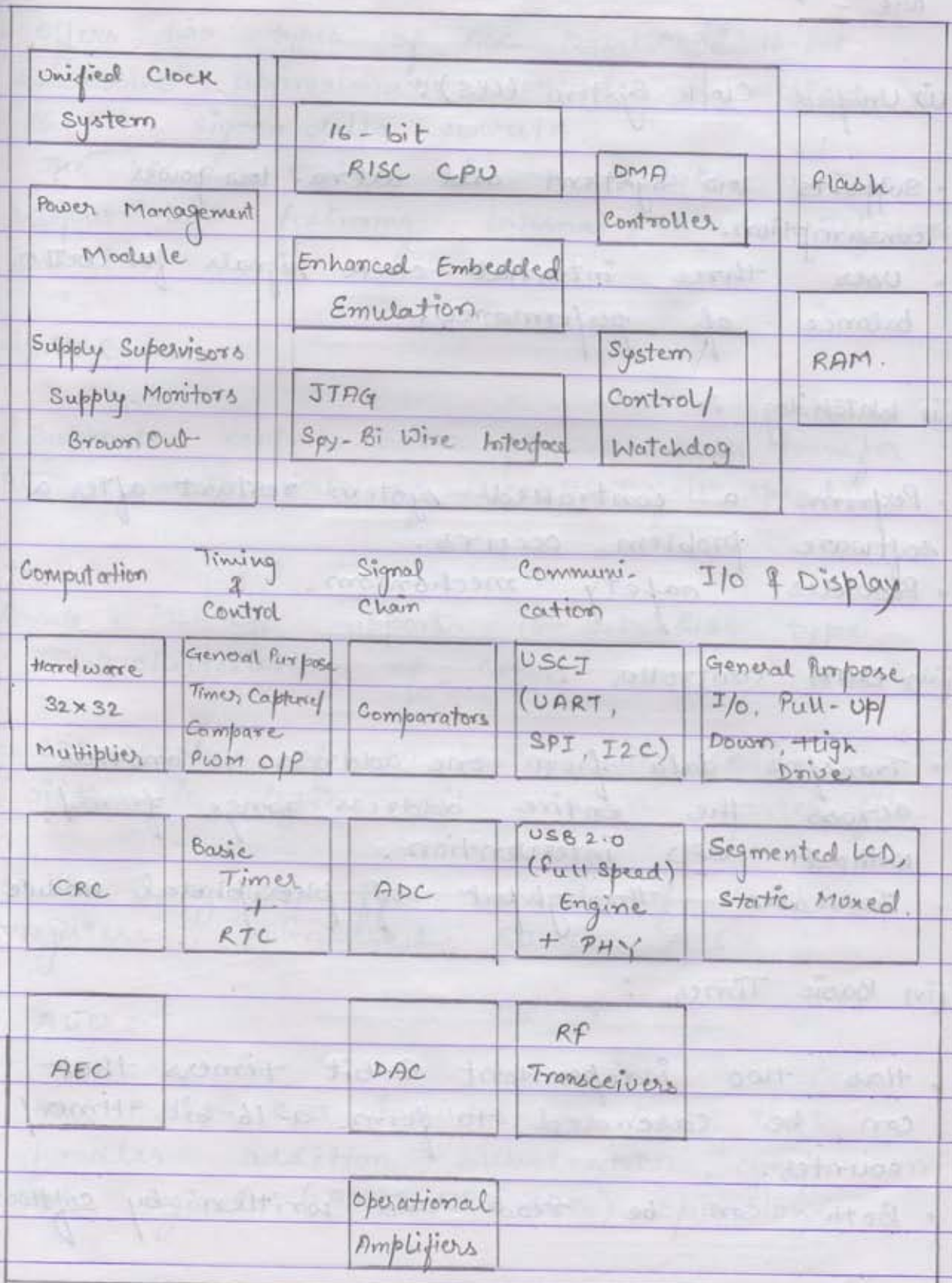
- The RAM address space from 20H to 2FH and some special function register are bit address able.

- For eg. – SETB 06H.

Ans. 2

Characteristics	CISC	RISC
Instruction Size	Varies	Fixed
Instruction Length	1, 2, 3 or 4 bytes	4 bytes.
Acronym	Complex Instruction Set Computers	Reduced Instruction Set computers.
No. of instruction	More	Less
Registers	Few, may be special purpose	Many. general purpose.
Instruction Execution Speed	Slow	Medium
Compiler	Simple	Complicated.
Addressing Modes	Support complex addressing modes.	Complex addressing modes are synthesized in software.
Pipelined	Not pipelined or less pipelined	Highly pipelined.
Examples	Intel X86, Motorola 68000, etc	ARM, 8051, ATMEL, etc.

Ans.3 MSP430x5xx Architecture :



Some of the important blocks of this architecture are -

(i) Unified Clock System (UCS):

- Supports low system and ultra-low power consumption.
- Uses three internal clock signals for better balance of performance.

(ii) Watchdog :

- Performs a controlled system restart after a software problem occurs.
- Provides safety mechanism.

(iii) DMA controller :

- Transfers data from one address to another across the entire address range ~~from~~ / without CPU intervention.
- Increases throughput of peripheral module.

(iv) Basic Timer :

- Has two independent 8-bit timers that can be cascaded to form a 16-bit timer / counter.
- Both can be read and written by software.

(v) ADC and DAC :

- Offers two types of ADC 10-bit and 12-bit successive approximation converter as well as 16-bit sigma delta converter.
- The DAC12 module is a 12-bit, voltage-output DAC featuring internal / external reference selection.

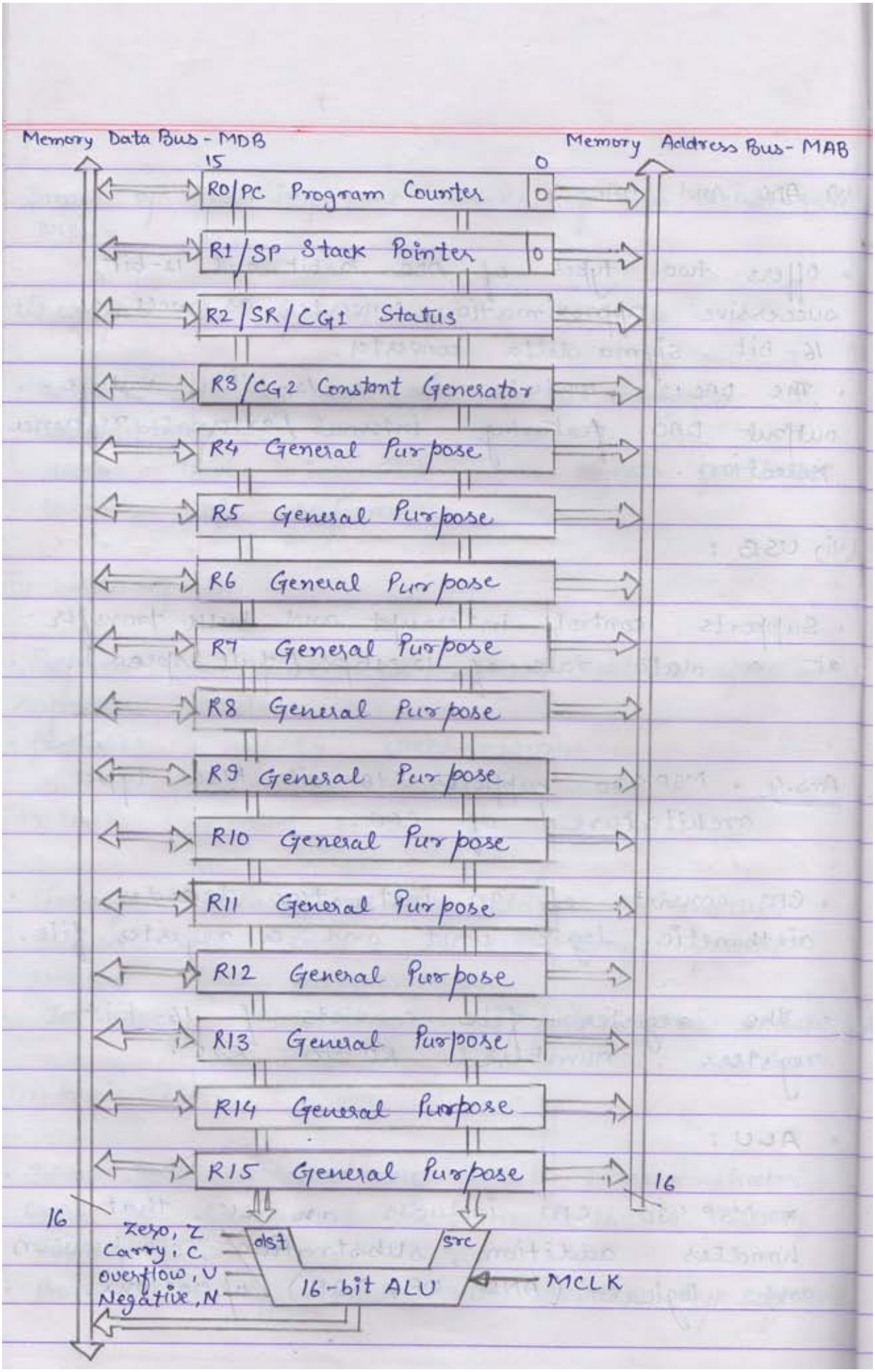
(vi) USB :

- Supports control, interrupt and bulk transfer at a data rate of 12 Mbps (full speed).

Ans.4 . MSP 430 supports 16-bit RISC type architecture of CPU.

- CPU consists of an instruction decoder, airthmetic logic unit and a register file.
- The register file consists of 16-bit registers, numbered R0 to R15.
- ALU :

  * MSP 430 CPU includes an ALU, that handles addition, substration, comparison and logical (AND, OR, XOR) operations.


Memory Data Bus - MDB
Memory Address Bus - MAB
15
0
R0/PC Program Counter
R1/SP Stack Pointer
R2/SR/CG1 Status
R3/CG2 Constant Generator
R4 General Purpose
R5 General Purpose
R6 General Purpose
R7 General Purpose
R8 General Purpose
R9 General Purpose
R10 General Purpose
R11 General Purpose
R12 General Purpose
R13 General Purpose
R14 General Purpose
R15 General Purpose
16
16
Zero, Z
Carry, C
Overflow, V
Negative, N
dst
src
16-bit ALU
MCLK

* R0 - Program Counter (PC) :

* Instruction are composed of 1-3 words, which must be aligned to even addresses, so the LSB of PC is hard-wired to 0.

• R1 - Stack Pointer (SP) :

* MSP430 uses R1 as pointer to stack in RAM.

* Stack Pointer points to last value pushed on stack.

* Values are pushed as 16-bit words and after that stack pointer is decremented by 2 and on pulling the value it get increased by 2.

• R2/R3 - Constant Generator :

* Depending on Source-register addressing mode, six commonly used constants can be generated without a code word or code memory access to retrieve them.

* Powerful features, which allows the implementation of emulated instruction.

* R2 and R3 provide a range of useful values by exploiting the CPU's addressing mode.

• R2 - Status Register :

* Used as status register which contains a set of flags (single bits).
* Most common flags are C, Z, N, and V which give information about result of last arithmetic or logical operation.

C → Carry Flag
Z → Zero Flag
N → Negative Flag
V → Overflow Flag.

• R4 - R15 - General Purpose Register :

* Used as source or destination operands for most of the MSP430 instructions.
* Presence of large no. of general purpose register allow programmers to minimize memory access and code size.

Ans.5 • Memory including RAM, Flash/ROM, information memory, SFR's & peripheral registers mapped into single, contiguous address space.

• MSP430 devices have similar memory map, differing only in size of the regions for RAM and code.

End: 0FFFH Start: 0FFE0H	Interrupt Vector Table	Word / Byte
End: 0FFDFH Start*: 0F800H	Flash / ROM	Word / Byte
01100H		
End*: 010FFH 0107FH Start: 01000H	Information Memory (Flash Device Only)	Word / Byte
End: 0FFFH Start: 0C00H	Boot Memory (Flash Device Only)	Word / Byte
End*: 09FFH 027FH Start: 0200H	RAM	Word / Byte
End: 01FFH Start: 0100H	16-bit Peripheral Modules	Word
End: 00FFH Start: 0010H	8-bit Peripheral Modules	Byte
End: 000FH Start: 0000H	Special Function Registers (SFR's)	Byte

- SFR's are memory-mapped registers with special dedicated functions, located at memory addresses from 0000H to 000FH.
- SFR are specific registers for Interrupts enable, Interrupt flags, module enable flag.

- All on-chip peripheral registers are mapped into memory, immediately after the SFR's.
- They provide main communication b/w CPU and peripheral and are of two types : byte-addressable and word-addressable.
- RAM is used for all scratchpad variables, global variable and the stack. Its final address depends on size of RAM starting from 0x0200H.
- Boot memory is only hard-coded ROM space in flash devices containing the bootstrap loader, which is used for programming of flash blocks, via a USART module.
- Information memory acts as onboard EEPROM, allowing critical variables to be preserved through power down.
- All code, tables and hard-coded constants reside in code memory which is contiguous.
- Interrupt vector are located at very end of memory space. The priority of the interrupt vector increases with the word address.

Ans.6 Addressing Modes Of MSP430 are -

(i) Register Mode :

- This uses one or two registers in CPU for moving of content.
- Most straight-forward addressing mode and is available for both source and destination.
- Syntax : MOV r_s, r_d
  where r_s is source register and r_d is destination register.
- For eg.- MOV R11, R12
  This instruction copies the content of R11 to R12.

(ii) Indexed Mode :

- In this mode, the address is formed by adding a constant base address to the contents of a CPU register; the value of register is not changed.
- For eg.- MOV 3(R8), 4(R6)
  Before execution of this instruction R8 = 01050H and R6 = 01080H. Then 01050H + 3 = 01053H and 01080H + 4 = 01084H,

since 3 and 4 are indexes. Therefore, the content of address 01053H is moved to 01084H.

(iii) Symbolic Mode :

- In this case the program counter PC is used as the base address, so the constant is the offset to the data from the PC.
- Useful for applications but it is highly specialized, such as boot loaders where the code runs from RAM rather than ROM.
- For eg. – MOV X(PC), Y(PC)
  The content of the source address (PC + X) is moved to destination address (PC + Y). Hence, the program counter is altered and continued with next instruction.

(iv) Absolute Mode :

- The constant in this form of indexed addressing is the absolute address of data.
- The MSP430 mimics this by using the

status register SR.

- Used for special function and pheripheral register, whose addresses are fixed in the memory map.

- For eg.- MOV &ED, &TO
  This instruction copies the contents of the source address ED to destination address TO. ED and TO are user defined labels.

(V) Indirect Register Mode :

- This is available only for the source and is shown by the symbol @ in front of register.

- For eg.- MOV @R10, 0(R11)
  Let R10 = 0FA55H and R11 = 002A5H.
  The content of 0FA55H is considered as an address from which the content is copied to 002A5H.

(Vi) Indirect Autoincrement Register Mode :

- Available only for the source and is shown by symbol @ in front of register with + sign after it.

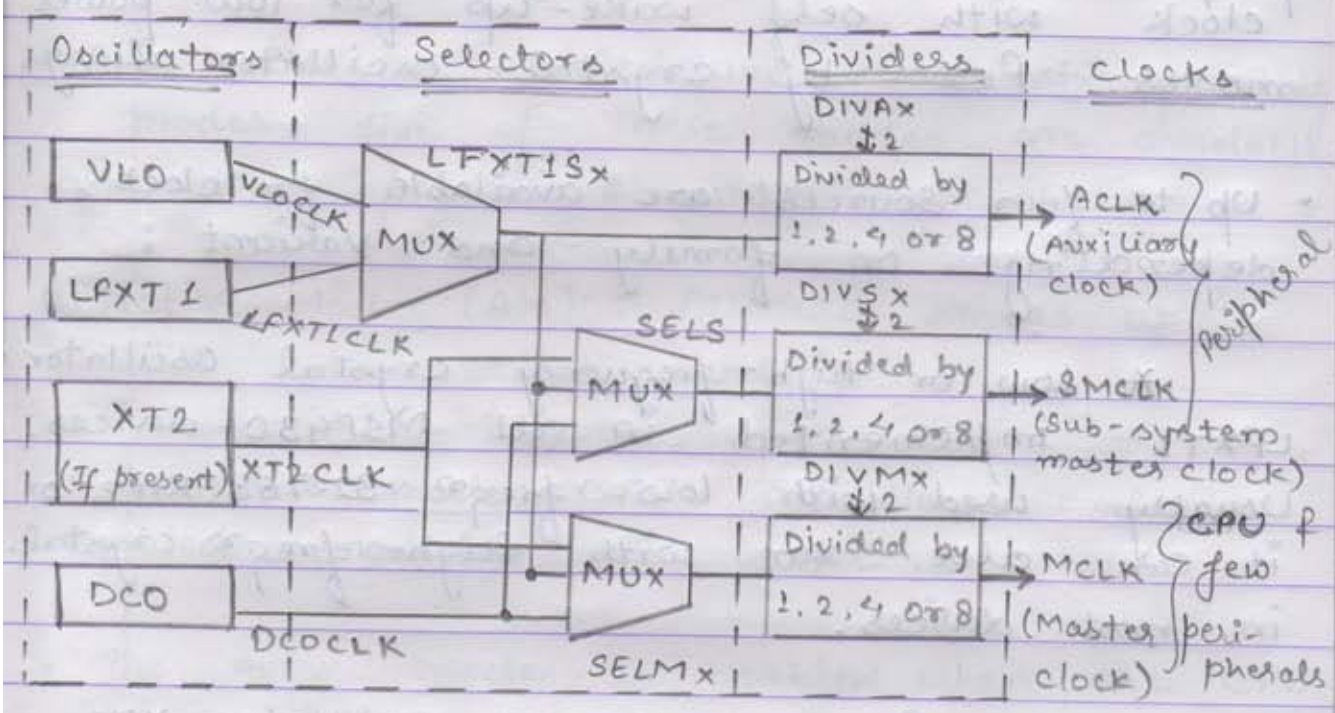
- Uses the value in reg. as pointer and automatically increments it afterward by 1 or 2 for byte or word fetched.
- For eg. - MOV @R10+, 0(R11)
  Let R10 = 0FA55H and R11 = 010A5H. The content 0FA55H is considered as an address from which the content is copied to 010A5H. Then R10 value 0FA55H is incremented by 1 for byte and by 2 for word.

(vii) Immediate Mode :

- Special case of autoincrement addressing that uses the program counter PC.
- Automatically PC is incremented after the instruction is fetched and therefore points to the following word.
- For eg. - MOV #45H, TO
  This instruction copies the immediate constant 45 to destination address specified by TO + it's content i.e., TO = 0FF16H and its content is 01192H, then 45 is copied to address (0FF16H + 01192H) resultant address.

Ans.7 • All microcontrollers contain a clock module to drive the CPU and pheripherals.

• MSP430 microcontroller have a clock system that allows the CPU and pheripherals to operate from different clock sources.



• Clock sources from these oscillators can be selected to generate a range of different clock signals :

* Master clock, MCLK used by CPU and few peripherals. Generated by Digitally controlled Oscillator (DCO) which can be activated and reach stability in less than 6μsec.

- * Sub-system master clk, SMCLK used as alternative clock source for ~~their~~ peripherals. It is in MHz range.

* Auxiliary clock, ACLK distributed to peripherals. It is background real-time clock with self wake-up for low power modes. Fed by crystal oscillator always.

- Up to four sources are available for clock, depending on family and variant:

* Low or high-frequency crystal oscillator LFXT1 implemented in all MSP430 devices. Usually used with low-freqn 32.768 KHz or it can also run with high-freqn crystal in most devices.

* High Frequency Crystal Oscillator, XT2 used in 1xx, 2xx and 4xx families as second crystal oscillator. Similar to LFXT1 except that it is restricted to Hf mode.

* Internal very low-power, low-frequency oscillator, VLO available only in MSP430f2xx devices. Provides alternative to LFXT1 when accuracy of crystal is not needed.

* Digitally Controlled Oscillator, DCO one of the highlights of MSP430. DCO highly controllable integrated ring RC oscillator able to provide a wide, software - controllable freqn range.

Ans.8 • MSP430 architecture allows six operating modes, five of these modes are available for low power consumption operation.

(i) Active Mode (AM) : MSP430 starts up with the active mode.

• In this mode, CPU, all clocks and enabled modules are active.

• The active mode is enabled when the CPU is required. The CPU is reactivated by an interrupt either internal or external.

(ii) LPM0 : Low-Power Mode-0.

• CPU and MCLK are disabled, SMCLK and ACLK remain active.

• Used when the CPU is not required but some modules require a fast clock from SMCLK and DCO.

(iii) LPM 1 : Low- Power Mode 1.

- Difference between LPM0 and LPM1 lies in the ability ~~to~~ of LPM0 to enable/ disable the DCO's DC generator, depending on peripherals used.

(iv) LPM 2 : Low - Power Mode 2

- In this, the DCO's DC generator remains active, even though the DCO is disabled.

- In this mode, ACLK is only thing running in the CPU, and it takes roughly one-tenth as much current as the DCO generator.

(v) LPM 3 : Low- Power Mode 3.

- Only ACLK is active.

- Standard low- Power mode. Provides lower power consumption periodic interrupt. capability.

(vi) LPM 4 : Low - Power Mode 4.

- LPM 4 useful for systems that use externally

generated interrupts only, as no clocks are active and available for peripherals.

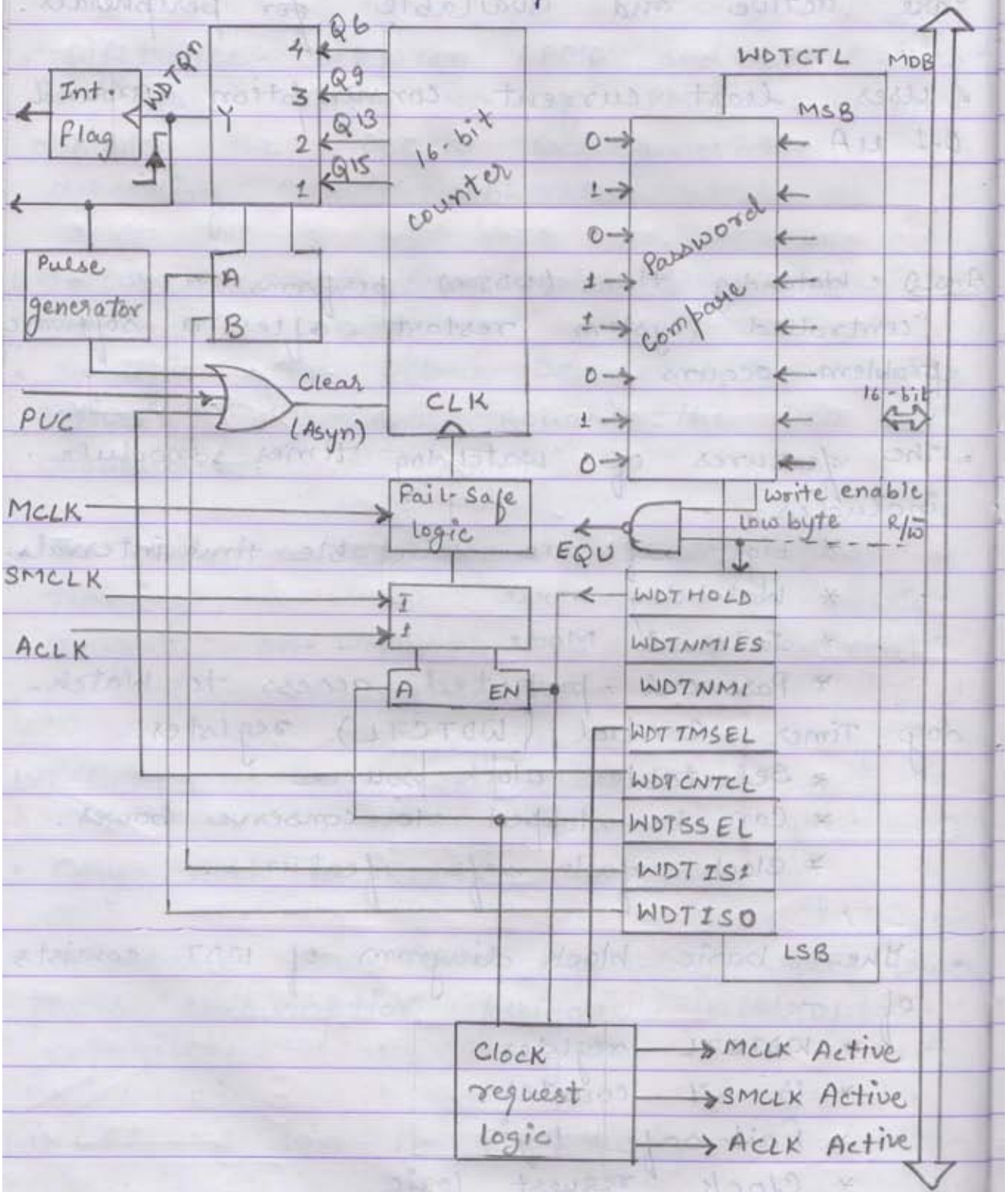
- Uses least current consumption, around 0.1 μA.

Ans.9 • Watchdog timer (WDT+) performs a controlled system restart after a software problem occurs.

- The features of watchdog timer module includes. –
  - * Eight software - selectable time intervals.
  - * Watchdog mode
  - * Interval Mode
  - * Password - protected access to Watch-dog Timer Control (WDTCTL) register.
  - * Selectable clock source
  - * Can be stopped to conserve power.
  - * Clock fail-safe features.

- The basic block diagram of WDT consists of –
  - * WDTCTL register.
  - * 16-bit counter.
  - * Fail-safe logic
  - * Clock request logic
  - * Pulse generator.

* Interrupt Flag.



• Two working modes of Watchdog Timer are –

* Watchdog Mode :

• After Power-Up Clear (PUC) condition, the WDT module is configured in the watchdog mode with an initial ~32 ms reset interval using the DCOCLK.

• When WDT is configured to operate in this mode, either writing to WDTCTL with an incorrect password, or expiration of the selected time interval triggers a PUC.

* Interval Timer Mode :

• Setting the WDTTMSEL bit in WDTCTL to 1 selects the interval timer mode.

• This mode can be used to provide periodic interrupts.

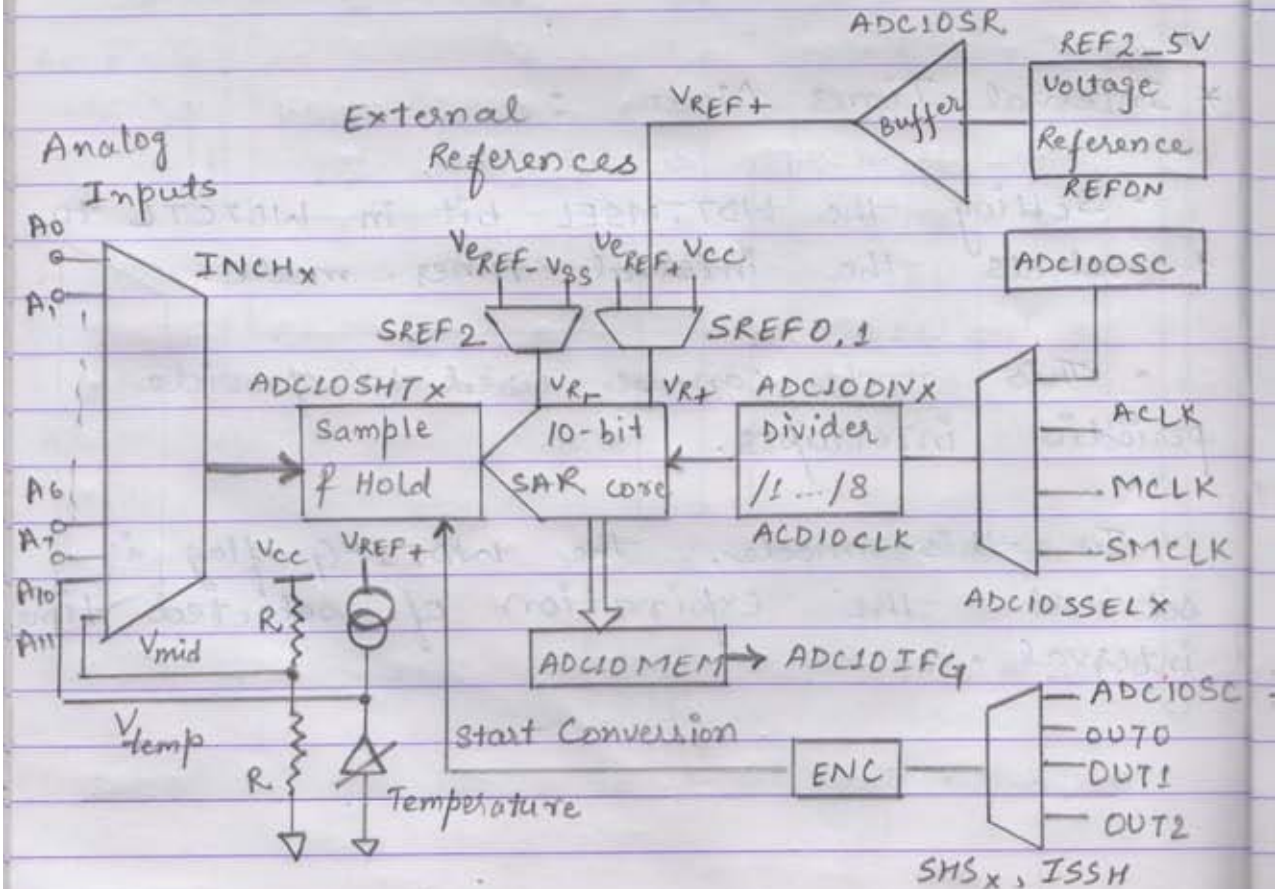
• In this mode, the WDTIFG flag is set at the expiration of selected time interval.

Ans.10 • There are two Successive-Approximation Register (SAR) ADC modules available on the MSP430, the ADC10 and ADC12.

• Features of ADC10 includes:

* Greater than 200 ksps max. conversion rate.
* Up to twelve external i/p channels.
* Conversion initiation by software or Timer_A.
* Sample-and-hold with programmable sample periods.

• The main section of the ADC10 is a 10-bit,



switched - capacitor, SAR core.

- The ADC10ON bit enables the core and a flag ADC10BUSY is set while sampling and conversion is in progress; the result is written to ADC10MEM.
- With ADC10SSELx bits, the clock can be taken from MCLK, SMCLK, ACLK or module's internal oscillator ADC10OSC.
- A multiplexer is used to select the input from eight external pins $A_0 - A_7$ and four internal connections.
- Two of internal connections are for operational, external reference voltages, which share the pins for A3 and A4 in many devices.
- The other two internal connections are A10 to temperature sensor and A11 to $V_{mid} = \frac{1}{2}(V_{cc} + V_{ss})$, which is provided to monitor the supply voltage.

Ans. 11 .. The comparator operation is controlled with two peripheral registers CACTL1 and CACTL2.

- Comparator_A Control Registes 1 (CACTL1)

7	6	5	4	3	2	1	0
CAEX	CARSEL	CAREF x		CAON	CAIES	CAIE	CAIFG

CAEX	Comparator_A exchange. This bit exchange the comparator i/p and invert the comparator o/p.
CARSEL	Comparator_A reference select. This bit selects which terminal the V_{CAREF} is applied to. When CAEX = 0 0 V_{CAREF} is applied to + terminal 1 V_{CAREF} is applied to - terminal When CAEX = 1 0 V_{CAREF} is applied to - terminal 1 V_{CAREF} is applied to + terminal.
CAREF	Comparator_A reference. These bits select the reference voltage V_{CAREF}. 00 Internal reference off. An ext. ref. applied 01 0.25 * V_{cc} 10 0.50 * V_{cc} 11 Diode reference is selected.
CAON	Comparator_A on. This bit turns on the comparator.

	0 Off 1 ON
CAIES	Comparator_A interrupt edge select 0 Rising edge 1 Falling edge.
CAIE	Comparator_A interrupt enable 0 Disabled 1 Enabled
CAIFG	Comparator_A interrupt flag. 0 No interrupt pending. 1 Interrupt pending.

- Comparator_A Control Register 2. (CACTL2)

7	6	5	4	3	2	1	0
Unused				P2CA1	P2CA0	CAF	CAOUT

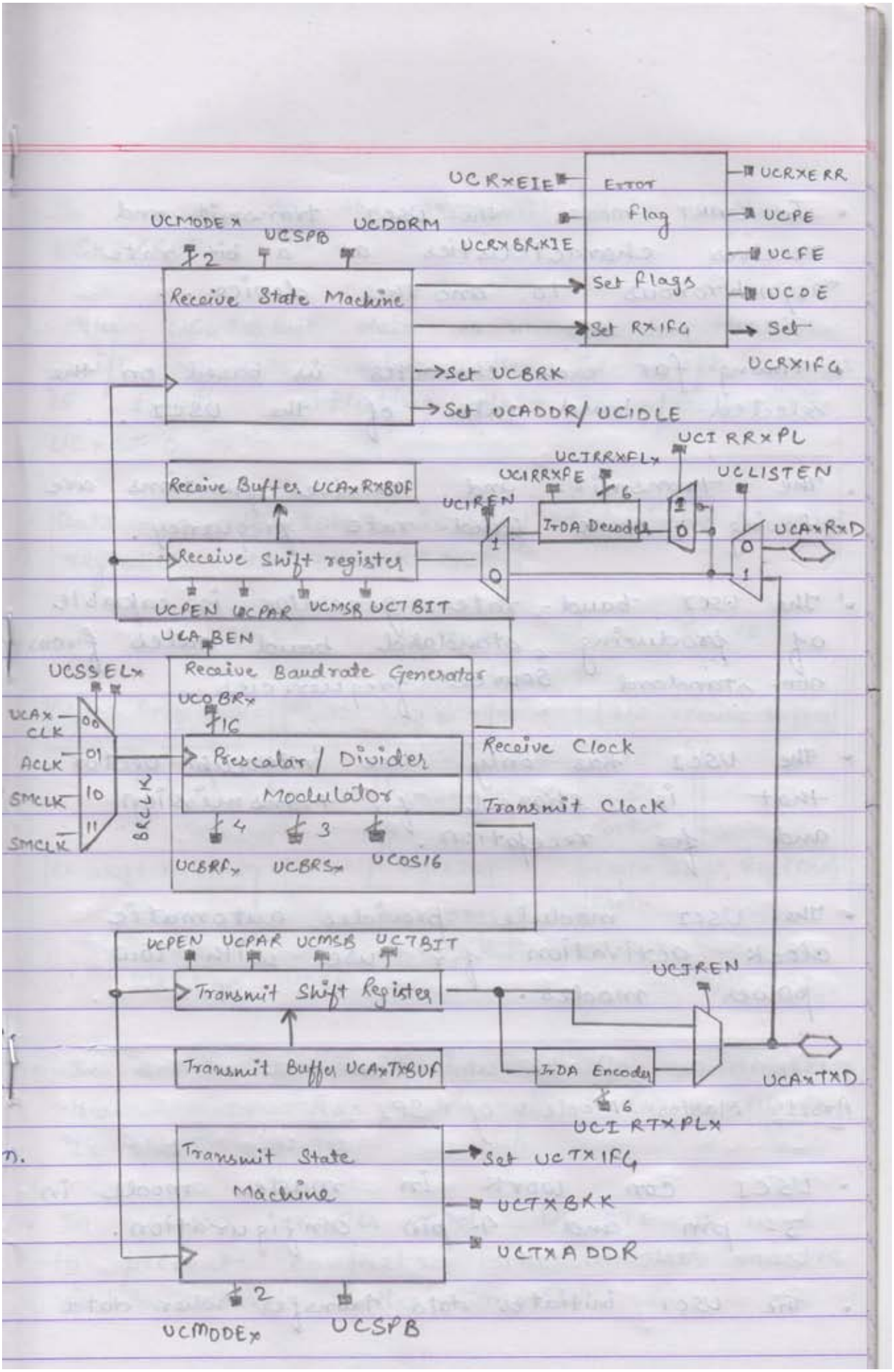
Unused	Unused.
P2CA1	Pin to CA1. Selects CA1 pin function 0 The pin is not connected to CA1 1 The pin is connected to CA1.
P2CA0	Pin to CA0. Selects CA0 pin function

	0 The pin is not connected to CA0 1 The pin is connected to CA0.
CAF	Comparator_A output filter 0 Comparator_A o/p is not filtered. 1 Comparator_A o/p is filtered.
CAOUT	Comparator_A output. This bit reflects the value of comparator output.

Ans. 13. In asynchronous mode, when the USCI_Ax control register bit 0 i.e., UCSYNC bit is cleared UART mode is selected.

- UART mode features includes :

* 7- or 8- bit data with odd, even or non-parity
* Independent transmit and receive shift register
* Separate transmit and receive buffer registers.
* Status flag for error detection and suppression.
* Status flag for address detection.
* Independent interrupt capability for receive and transmit.


UCRXEIE
Error
Flag
UCRXERR
UCPE
UCFE
UCOE
Set UCRXIFG
UCMODEx
UCSPB
UCDORM
UCRXBRKIE
2
Receive State Machine
Set flags
Set RXIFG
Set UCBRK
Set UCADDR/UCIDLE
UCIRRXPL
UCIRRXFLx
UCIRRXPE
6
UCLISTEN
UCIREN
IrDA Decoder
UCAxRXD
Receive Buffer UCAxRXBUF
Receive Shift register
UCPEN UCPAR UCMSB UCTBIT
UCABEN
UCSSELx
Receive Baudrate Generator
UCOBRx
16
UCAx CLK
ACLK
SMCLK
SMCLK
00
01
10
11
BRCLK
Prescalar / Divider
Modulator
Receive Clock
Transmit Clock
4
3
UCBRFx
UCBRSx
UCOS16
UCPEN UCPAR UCMSB UCTBIT
Transmit Shift Register
UCIREN
Transmit Buffer UCAxTXBUF
IrDA Encoder
UCAxTXD
6
UCIRTXPLx
Transmit State Machine
Set UCTXIFG
UCTXBRK
UCTXADDR
2
UCMODEx
UCSPB

- In UART mode, the USCI transmit and receives characteristics at a bit rate asynchronous to another device.
- Timing for each character is based on the selected baud rate of the USCI.
- The transmit and receive functions are having same baud-rate frequency.
- The USCI baud-rate generator is capable of producing standard baud rates from non-standard source frequencies.
- The USCI has only one interrupt vector that is shared for transmission and for reception.
- The USCI module provides automatic clock activation for use with low power modes.

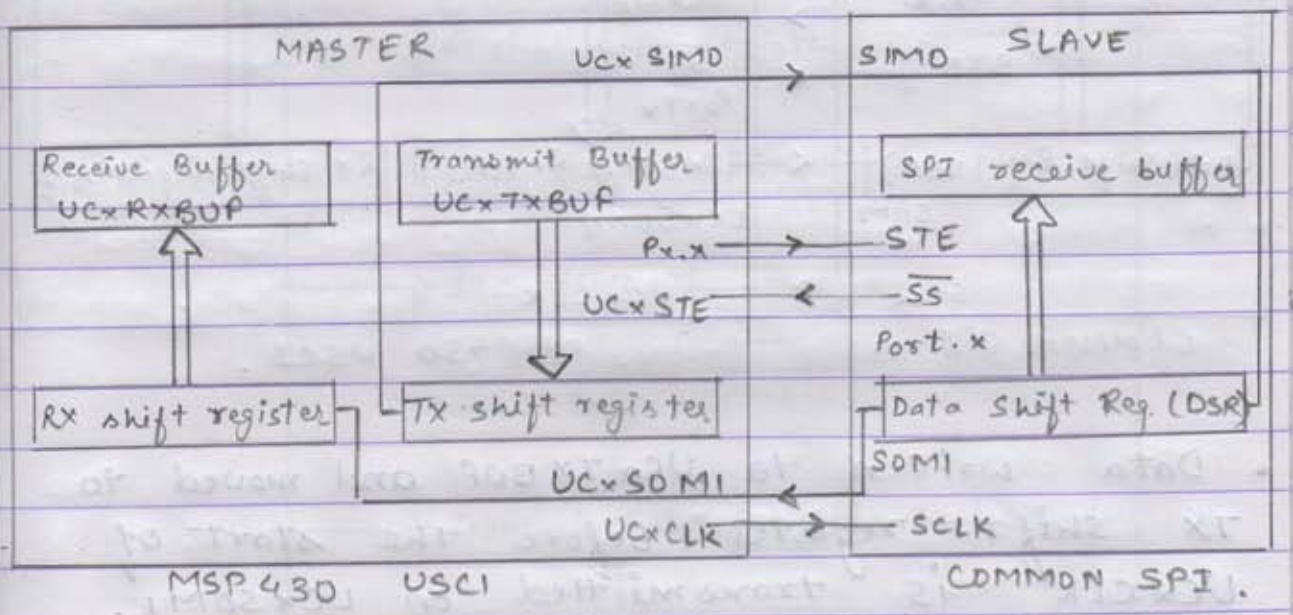
Ans.14 Master Mode of SPI.

- USCI can work in master mode in 3-pin and 4-pin configuration.
- The USCI initiates data transfer when data

is moved to the transmit data buffer UCxTXBUF.

- The UCxTXBUF data is moved to the TX shift register when the Tx shift register is empty, initiating data transfer on UCxSIMO.

- Data on UCxSOMI is shifted ~~from~~ the Rx shift register to UCxRXBUF.

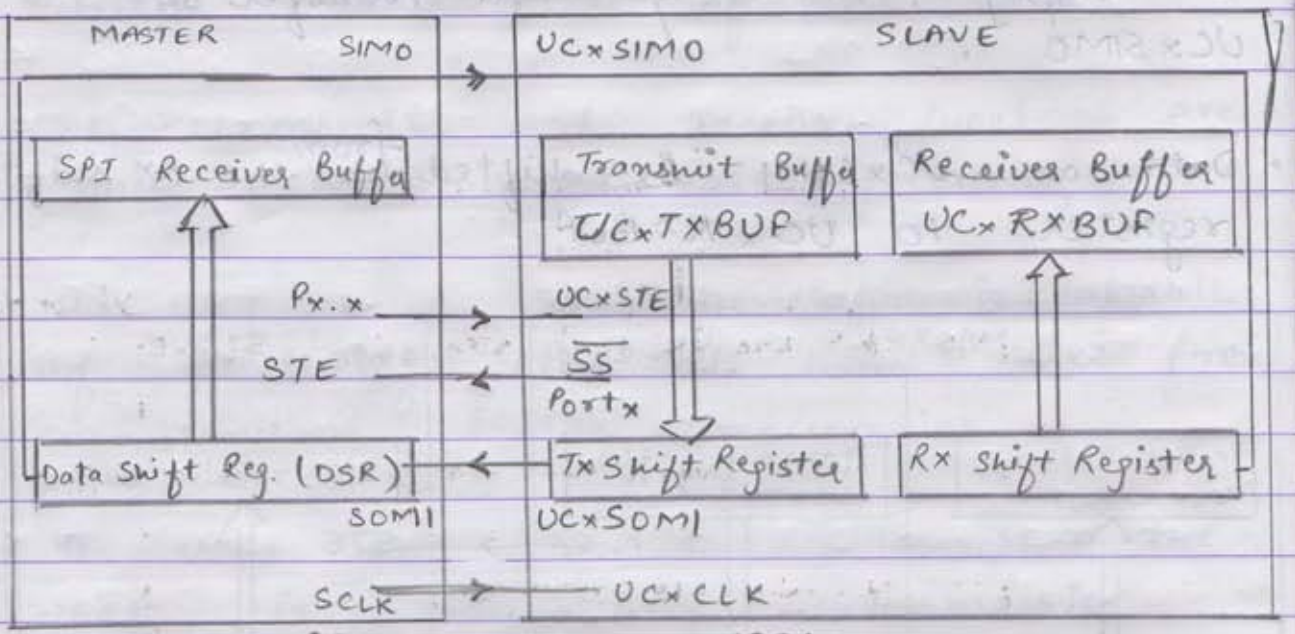


- ~~In~~ A set transmit interrupt flag, indicates that data has moved from UCxTxBUF to Tx shift register.

- In 4-pin master mode, UCxSTE is used to prevent conflicts with another master and controls the master.

Slave Mode Of SPI

- In this mode, UCxCLK is used as the input for SPI clock and must be supplied by external master.



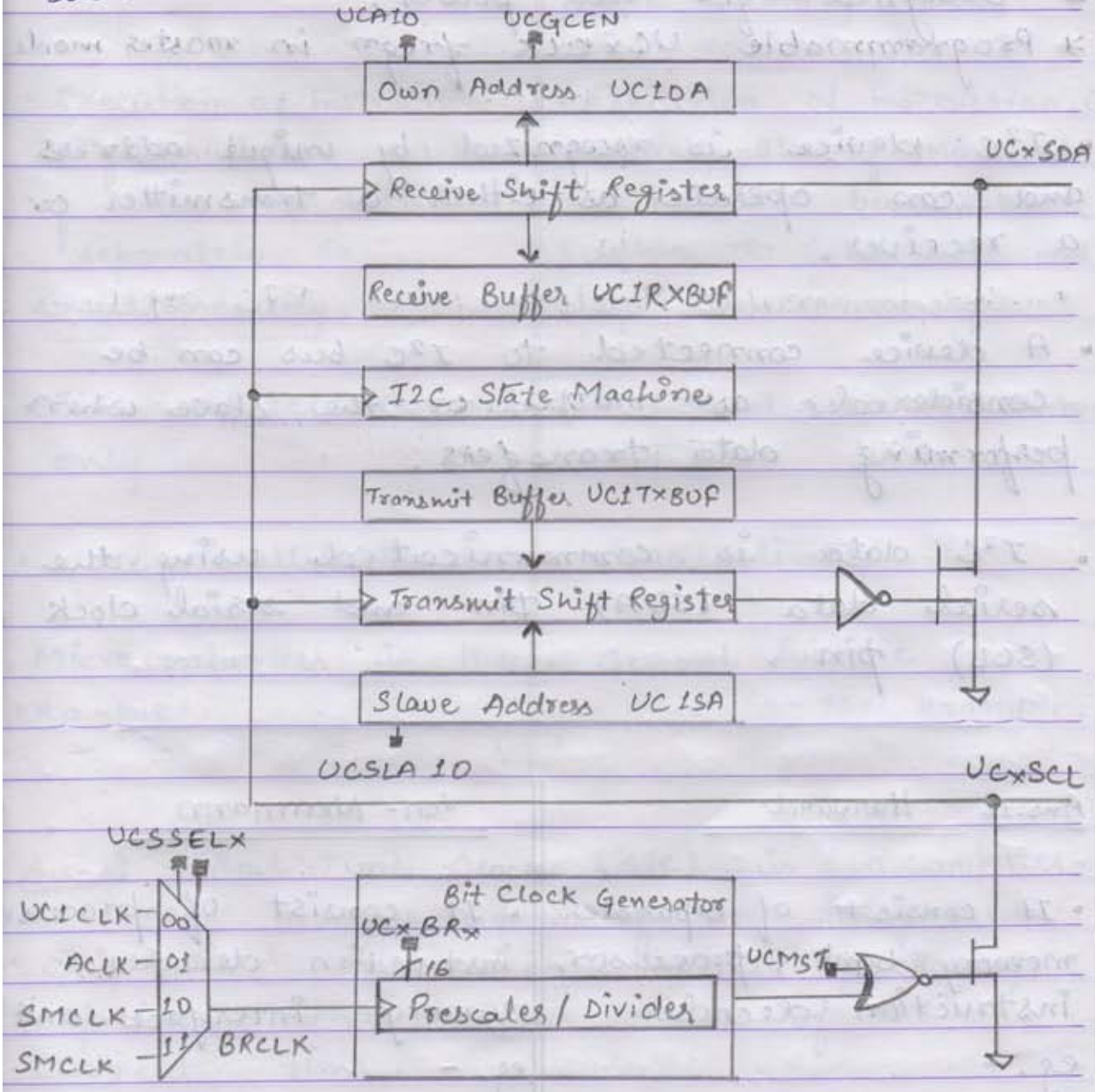
- Data written to UCxTXBUF and moved to TX shift register before the start of UCxCLK is transmitted on UCxSOMI.

- Data on UCxSIMO is shifted on the receive shift register on the opposite edge of UCxCLK and moved to UCxRXBUF when the set no. of bits are received.

- When the data is moved from the Rx shift register to UCxRXBUF, the

UCRXIFG interrupt flag is set, indicating that data has been received.

Ans. 15 . In I^2C mode, USCI module provides an interface btw the device & I^2C compatible devices connected by two-wire I^2C serial bus.



- I^2C mode features include :

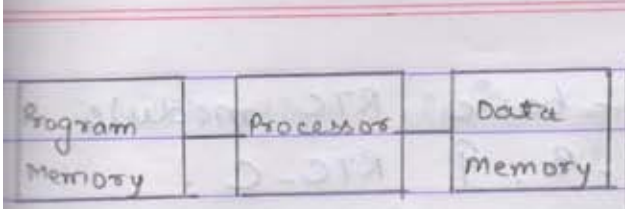
* 7- bit and 10- bit device addressing modes.
* START / RESTART / STOP .
* Multi - master transmitter / receiver mode.
* Slave receiver / transmitter mode.
* Slave operation in LPM4.
* Designed for low powers.
* Programmable UCx CLK freqn in master mode

- I^2C device is recognized by unique address and can operate as either a transmitter or a receiver.

- A device connected to I^2C bus can be considered as master or the slave when performing data transfers.

- I^2C data is communicated using the serial data (SDA) pin and serial clock (SCL) pin .

Ans.16 Harvard	Von- Neumann
• It consist of separate memory bank , processor, instruction decode. eg. -	• It consist of processor instruction decoder, memory interface unit eg. -



• This architecture consist of separate code (program) and data memory.	• This architecture consist of memory i.e., program (code) and data used same memory area.
• Execution of instruction is faster becoz fetching of code and data separately or simultaneously.	• Execution of instruction is relatively slow of Harvard architecture bcoz not possible to fetch code and data simultaneously.
• RISC architecture used only	• RISC and CISC architecture only.
• More Parallelism	• Parallelism.
• Micro controller is the example.	• General Purpose Microprocessor is the example.

Ans-18 • Real Time Clock (RTC) is a computer clock in the form of an integrated chip (IC) available in various packaging options that keeps track of the current time.

- MSP430 provides 3 - basic RTC module. Namely RTC_A, RTC_B, & RTC_C.

(i) RTC_A features include :

- Configurable for real - time clock with calendar function or general - purpose counter
- Interrupt capability.
- Selectable BCD or binary format in RTC mode.
- Programmable alarms in RTC mode.
- Calibration logic for time offset correctio in RTC mode.

(ii) RTC_B features include :

- Real - time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, month & year.
- Interrupt capability.
- Selectable BCD or binary format.
- Programmable alarms.

- Calibration logic for time offset correction.
- Operation in LPM 3.5.

(iii) RTC-C features include :

- Real-time clock and calendar mode.
- Protection for real-time clock register
- Interrupt capability.
- Real-time clock calibration for crystal offset error.
- Real-time clock compensation for crystal temperature drift.
- Operation in LPM 3.5.

Ans. 19 • The DMA controller has six transfer modes selected by the DMADTx bits.

- Each channel is individually configurable for its transfer mode.
- The transfer mode is configured independently from the addressing mode.

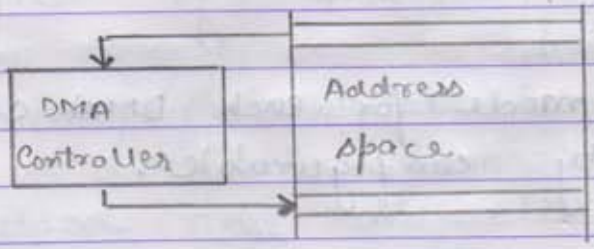
• DMA transfer modes –

DMADTx	Transfer Mode	Description
000	Single Transfer	• Each byte/word transfer requires a separate trigger. • The DMAxSZ register is used to define the no. of transfers to be made. • DMAEN is automatically cleared when DMAxSZ transfers have been made.
001	Block Transfer	• A complete block is transferred with one trigger. • DMAxSZ register is used to define the size of block. • DMAEN is automatically cleared at the end of the block transfer.
010, 011	Burst - block Transfer	• CPU activity is interleaved with a block transfer. • DMAxSZ reg. used to define size of block. • DMADSTINCRx & DMASRCINCRx bits select for increment or decrement

		of destination and source address after each transfer of block.
100	Repeated Single Transfer	• Each transfer requires a trigger. • DMAEN remains enabled.
101	Repeated Block Transfer	• A complete block is transferred with one trigger. • DMAEN remains enabled.
110, 111	Repeated Burst - Block Transfer.	• CPU activity is interleaved with a block transfer. • DMAEN remains enabled.

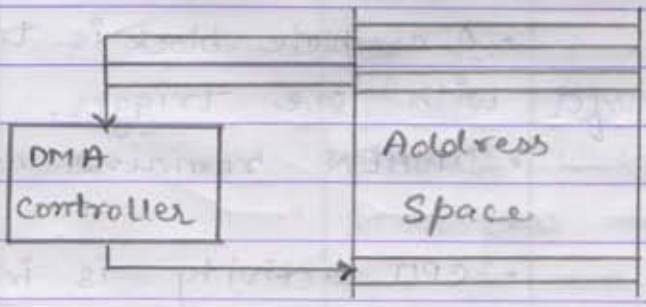
• The addressing modes of DMA controller are -

(i) Fixed address to fixed address

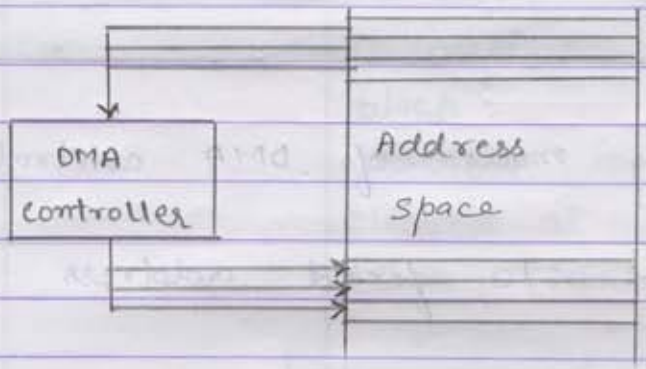


(ii) Fixed address to block of address

(iii) Block of address to fixed address



(iv) Block of addresses to block of addresses



- The addressing mode for each DMA channel is independently configurable.
- The addressing modes are configured with DMASRCINCRx and DMADSTINCRx control bit in the DMA channel

Control Register.

- For example, channel 0 may transfer between two fixed addresses, while channel 1 transfers btw two blocks of address.

~~Ans. 21~~ Ans. 20

- One of the most important interfaces between the MSP430 micro-controller and the real world is the Analogue-to-Digital converter (ADC).

- This allows a digital representation of a physical signal to be measured, usually an electrical signal and measured in volts.

- The first stage in this process is often amplified of analogue signal.

- The amplified signal is then converted into a digital form that can be processed by an electric circuit.

- When the analogue electrical signal is conditioned to be compatible with the

range of values supported by ADC, the conversion operation initiates a sample-and-hold function.

- The time interval between samples should be based on Nyquist theorem, so that the analogue signal is converted into digital signal that reproduces all its amplitude variation.

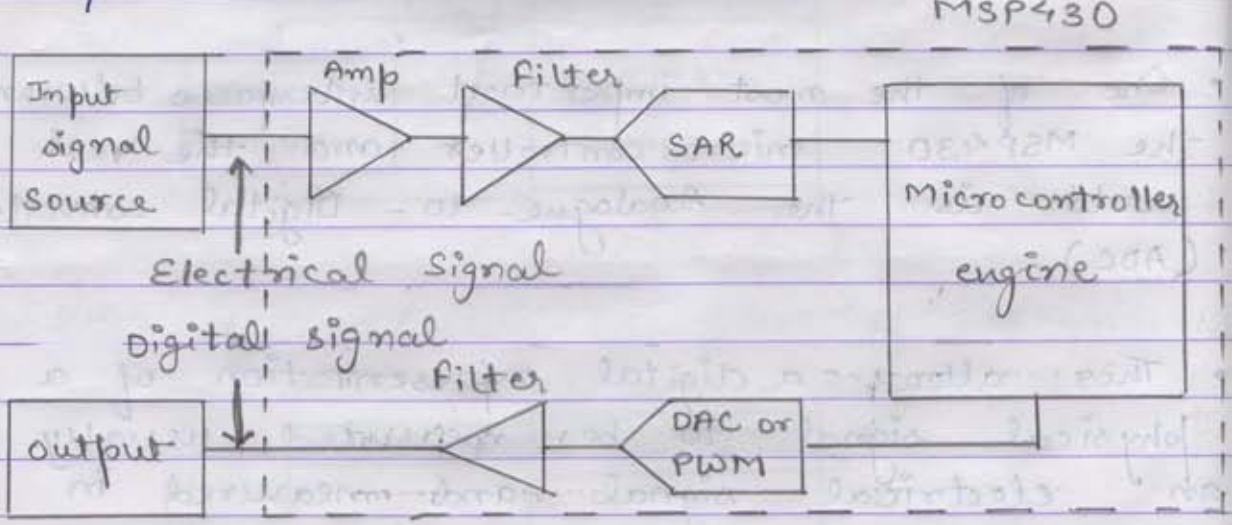


Fig. - Schematic Diagram of data acquisition system using MSP430.

- The output value of the sample-and-hold is fed into the ADC, which generates a digital code that can be used by a digital processing system

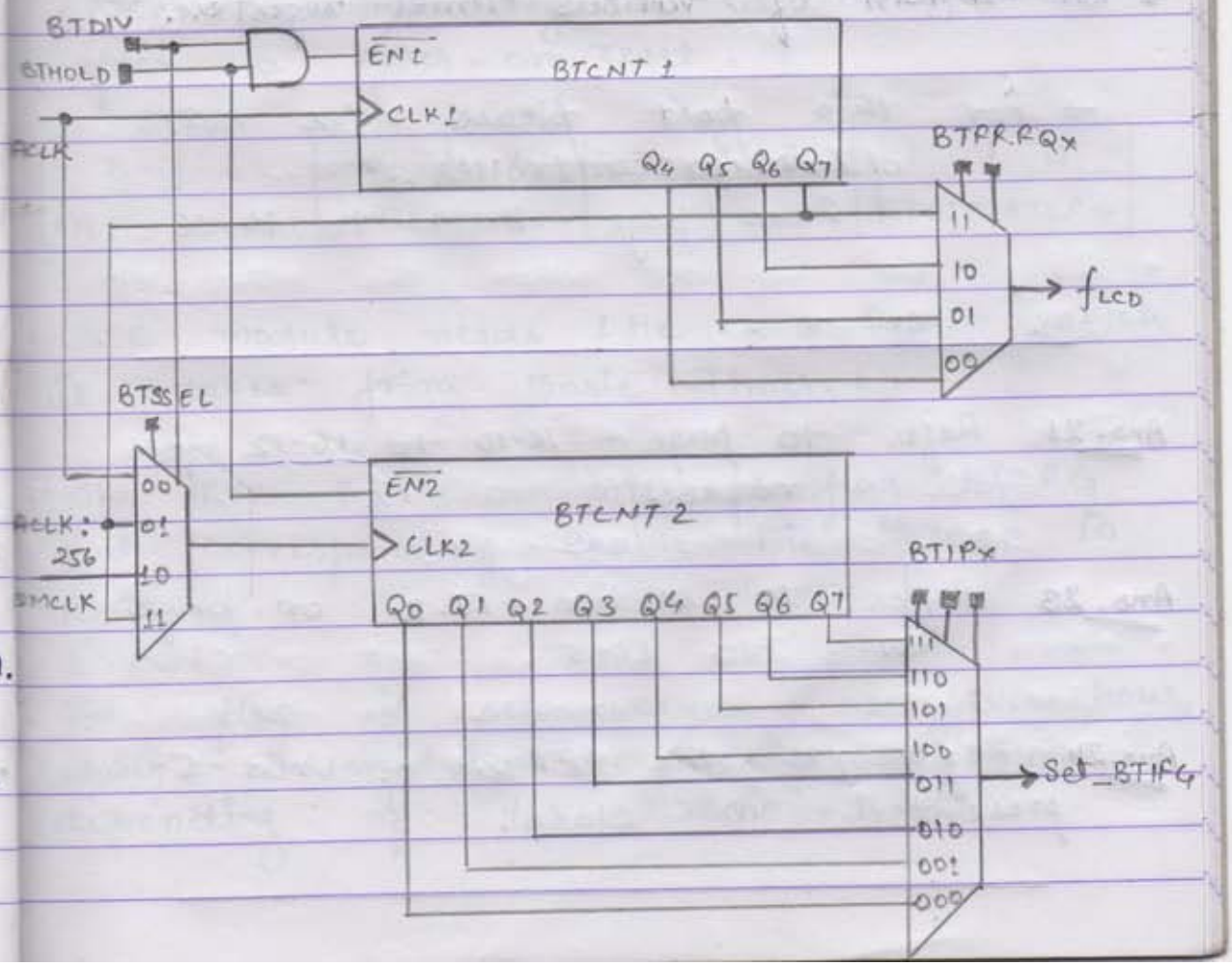
- Several MSP430 devices include on-chip the signal conditioning the analogue-to-

digital converters.

Ans. 22 • The Basic Timer_1 supplies LCD timing and low frequency time intervals.

• Basic Timer_1 features include :

* Selectable clock source
* Two independent, cascadable 8-bit timer.
* Interrupt capability
* LCD control signal generation.



- The Basic Timer_1 module can be configured as two 8-bit timers or one 16-bit timer with the BTCTL register.
- The Basic Timer_1 controls the LCD frame frequency with BTCNT1
- BTCNT1 is incremented with ACLK and provides the frame frequency for the LCD controller and can be stopped by setting the BTHOLD and BTDIV bits.

* Bit Pattern of various timer register.

→ For this part please refer notes of Microcontroller from page - 14.14 to 14-16.

Ans. 21 Refer to page - 16-10 to 16-12 of notes.

Ans. 23 Refer to section - 17.2 or page 17-3 to 17-5.

Ans. 24 Refer to the PPT's of Unit-5 presented in class.

→ Draw the block diagram of RTC_A module.

Ans.17 • RTC_A module provides a real-time clock and calendar function that can also be configured as a general-purpose counter.

• Has a 32-bit counter, to automatically control the clock calendar. It counts seconds, minutes, hours, days, months and years.

• It is configured in calendar mode by setting RTCMODEx = 11 in control register RTCCTL.

• Bit pattern of Real-Time Clock Control Register. (RTCCTL). This register is initialized after a power-on reset.

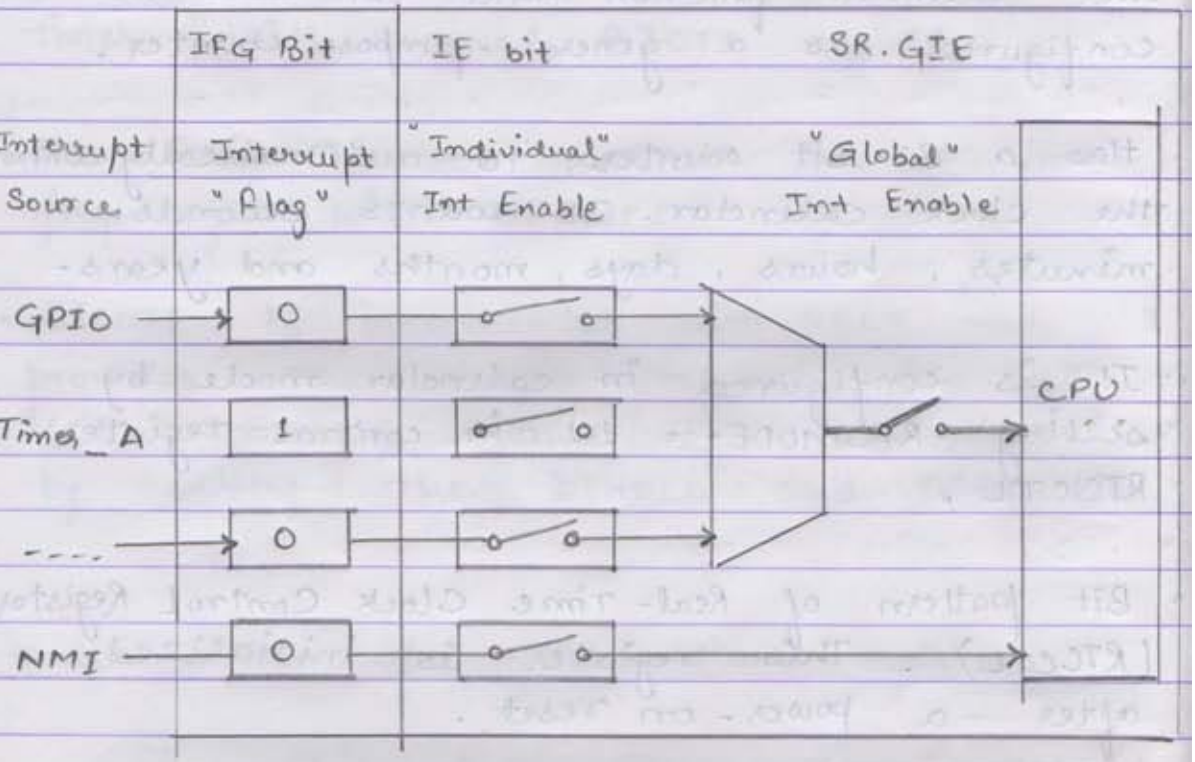
7	6	5	4	3	2	1	0
RTCBCD	RTCHOLD	RTCMODEx		RTCTEVx		RTCIE	RTCFG

• RTC module needs 1 Hz clock input, which it takes from Basic Timer_1.

• The RTC has an interrupt flag RTCFG and corresponding enable bit RTCIE in RTCCTL.

• The flag is set every minute, every hour, daily at midnight or daily at noon depending of the RTCTEVx bits.

Ans.12



Interrupt Flow Diagram.

- IFG bit is set when the interrupt gets occur.
- IFG bit can be set or cleared by eg.-
  GPIO_getinterruptStatus()
  GPIO_clearinterruptflag().
- When the IFG bit is set or cleared, Interrupts get enabled or disabled individually by IE bit.

- For enabling of all maskable interrupts GIE pin or Global Interrupt Enable is set.

- For eg.- Enable :- bis_SR_register
  Disable :- bic_SR_ registes.

- The MSP430 supports a Non-maskable interrupt (NMI). This interrupt is not disabled by the GIE bit. It's main used for critical external system events.