Solution Subject : Digital System Design Subject Code : KEC302

B.Tech. 3rd SEMESTER SECOND SESSIONAL EXAMINATION, ODD SEMESTER, (2019-2020)

Branch : Electronics & Communication Engineering

Time –1hr 30 min Maximum Marks – 30

SECTION - A

Q-1) Attempt ALL parts- (5*1 = 05)

a) How many Flip-Flops are required for mod–16 counter?

Answer : The number of flip-flops required for Mod-16 Counter is 4.

b) Name the fastest logic. Justify your answer.

Answer : ECL is the fastest logic family of all logic families. (High speeds are possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated.

c) Define FPGA

Answer : A field-programmable gate array (**FPGA**) is an integrated circuit designed to be configured by a designer.

d) What is the difference between PLA and PAL

Answer : The significant difference between the PLA and PAL is that the PLA consists of the programmable array of AND and OR gates while PAL has the programmable array of AND but a fixed array of OR gate

e) What is a flip-flop?

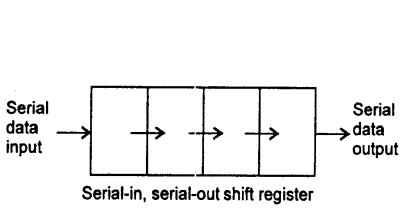
Answer : Flip-Flop: A flip-flop is a basic memory element used to store one bit of information. Both Flip-flops and latches are bistable logic circuits.

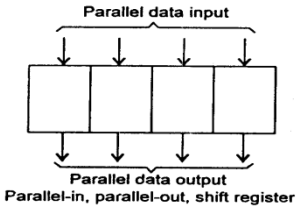
SECTION - B

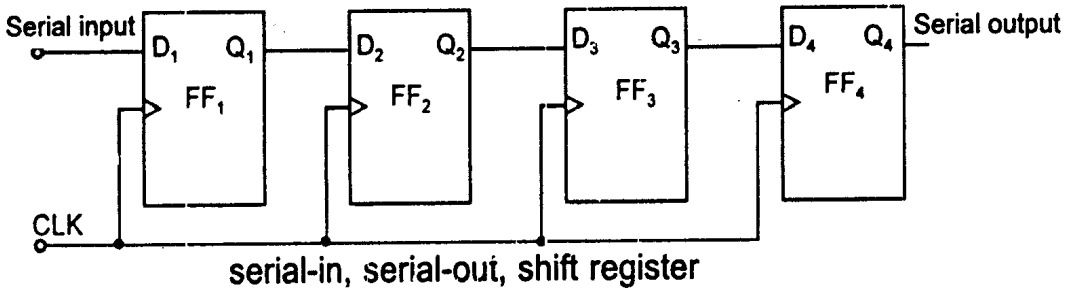
Q 2) Attempt any TWO parts from this section. (2*5 = 10)

a. Draw the logic circuit of SISO and PIPO shift register. Explain operation of PIPO shift register.

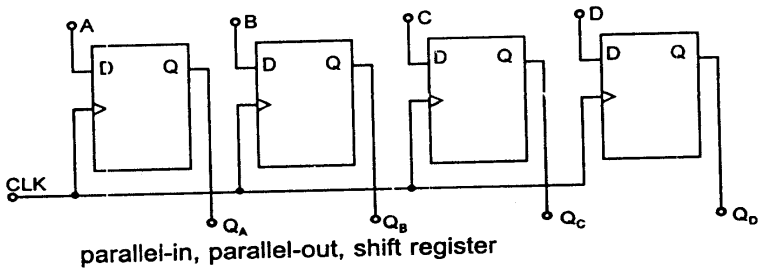
Answer :







serial-in, serial-out, shift register

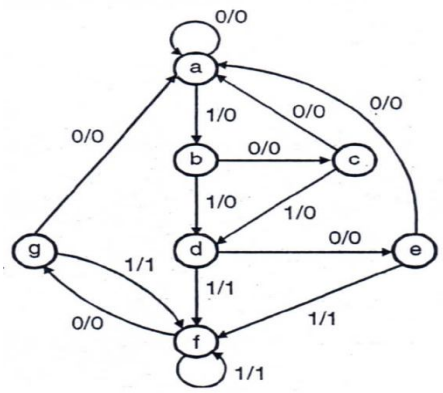


parallel-in, parallel-out, shift register

Operation : In a parallel-out, shift register, the data is entered into the register in parallel form, and also the data is taken out of the register in parallel form. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.

A 4-bit parallel-in, parallel-out, shift register using D FFs. Data is applied to the D input terminals of the FFs. When a clock pulse is applied, at the positive- going edge of that pulse, the D inputs are shifted in to the Q outputs of the FFs. The register now stores the data. The stored data is available instantaneously for shifting out in parallel form.

b. Draw the reduced state table and state diagram for the state diagram given below.



Answer

Step 1 : Write the state table from the given state diagram.

Step 2 : Identify the equivalent states.

Step 3 : Eliminate one of the two equivalent states and write a new state table.

Step 4 : In the new state table, check for equivalent states and continue till all the redundant state are eliminated.

Step 5 : Draw the state diagram

Step 1 : Write the state table :

State table

Present state	Next state		Output Y	
	X = 0	X = 1	X = 0	X = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Step 2 : Identify the equivalent states :

States "e" and "g" are equivalent states

Step 3 : Eliminate one of the equivalent states and write a new state table :

Modified state table with state reduction

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	~~g~~ e	f	0	1

After replacing "g" by "e" the states "d" and "f" have become equivalent.

State "g" has been eliminated

"g" is replaced by "e"

Step 4 : Replace "f" by "d" and prepare a new state table :

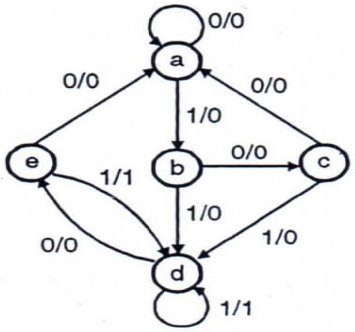
Reduced state table

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	~~f~~ d	0	1
e	a	~~f~~ d	0	1

"f" is replaced by "d"

State "f" has been eliminated

Step 5 : Draw the state diagram :



Reduced state diagram

c. Show how the FPLA circuit can be programmed to implement the 3 bit Binary to Gray conversion.

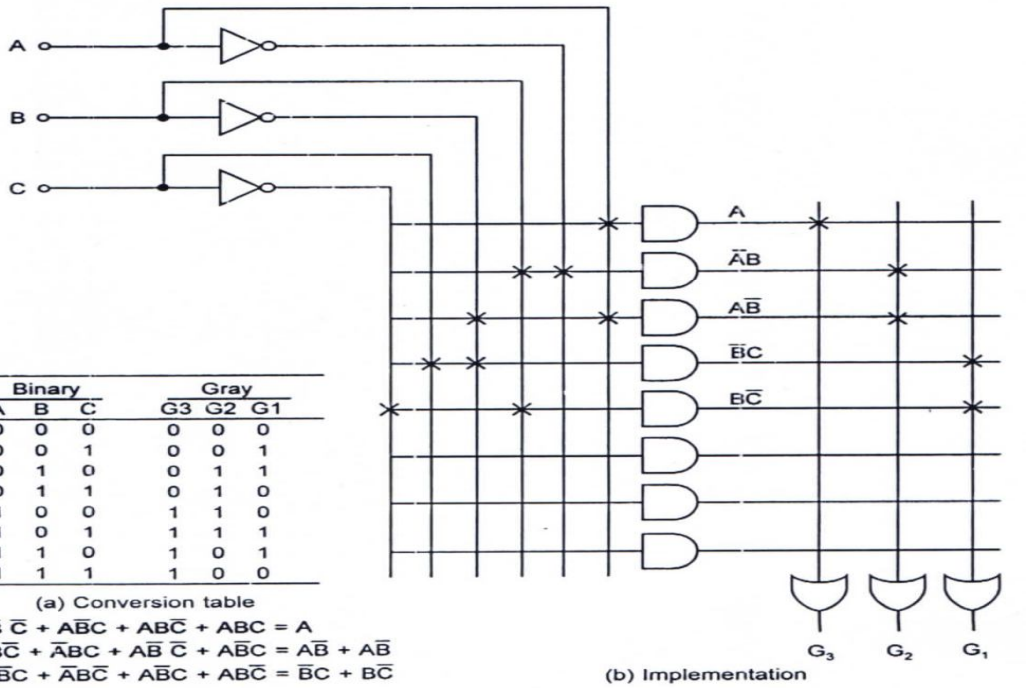
Answer :

The conversion table of 3-bit binary (A, B, C)-to-gray (G_3, G_2, G_1) is shown in Fig.

The conversion equations, $G_3 = A$

$G_2 = A\overline{B} + \overline{A}B$

$G_1 = B\overline{C} + \overline{B}C$ are implemented



Binary			Gray		
A	B	C	G3	G2	G1
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

(a) Conversion table

(b) Implementation

$G_3 = A\overline{B}\,\overline{C} + A\overline{B}C + AB\overline{C} + ABC = A$

$G_2 = \overline{A}BC + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C = A\overline{B} + \overline{A}B$

$G_1 = \overline{A}\,\overline{B}C + \overline{A}BC + A\overline{B}C + ABC = \overline{B}C + B\overline{C}$

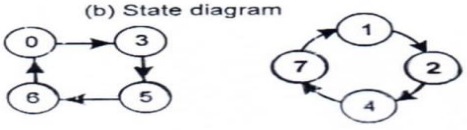
d. Design a type T counter that goes through states 0,3,5,6,0……

Answer :

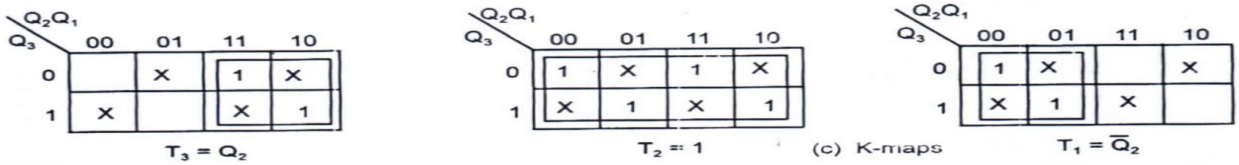
PS			NS			Required excitation		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	0	1	1	0	1	1
0	1	1	1	0	1	1	1	0
1	0	1	1	1	0	0	1	1
1	1	0	0	0	0	1	1	0

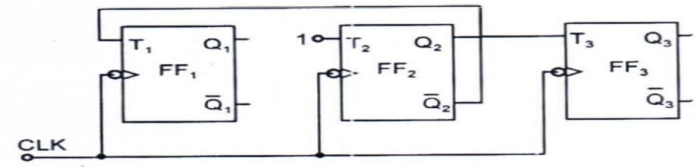
(a) Excitation table

(b) State diagram



(c) K-maps





Logic diagram T type, 0, 3, 5, 6, 0... counter

SECTION - C

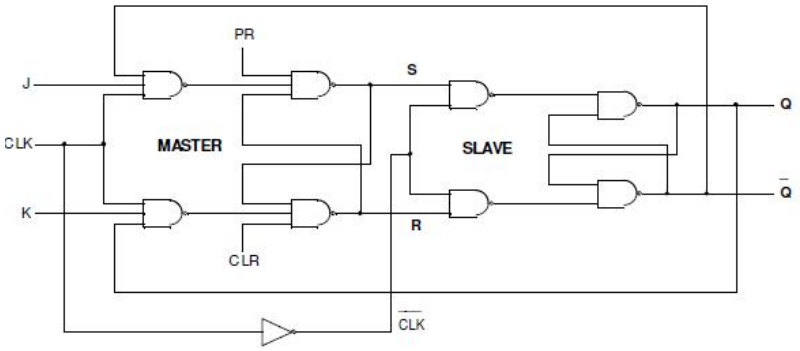
3. Attempt any ONE part of the following : (1*5 = 5)

a) With relevant diagram explain the working of master-slave JK flip flop.

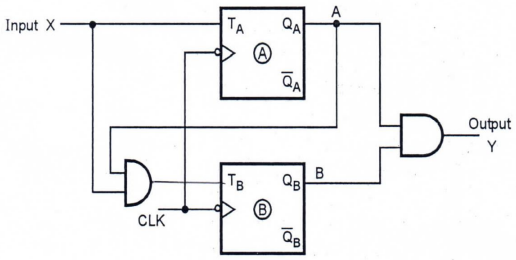
Answer : Master-Slave *J-K* FLIP-FLOP: A master-slave *J-K* FLIP-FLOP is a cascade of two *SR* FLIP-FLOPS. One of them is known as Master and the other one is slave. The master is positively clocked. Due to the presence of inverter, the slave is negatively clocked. This means that when clock is high, the master is active and the slave is inactive.

When the clock is low, the master is inactive and the slave is active.

This is a level clocked Flip-Flop. When clock is high, any changes in J and K inputs can affect S and R outputs. Therefore, J and K are kept constant during positive half of clock. When clock is low, the master is inactive and J and K inputs can be allowed to be changed. The different conditions are Set, Reset, and Toggle. The race condition is avoided because of feedback from slave to master and the slave being inactive during positive half of clock.



b) Write the input and output equation, obtain the state table and draw the state diagram for the synchronous sequential circuit shown in figure.



Answer

Step 1 : Input equations : $T_A = X$

$T_B = A \cdot X$

Output equation : $Y = A \cdot B$

Step 2 : Write the state table :

Table : State table

Present state		Input	Flip flop inputs		Next state		Output
A	B	X	$T_A = X$	$T_B = AX$	A_{n+1}	B_{n+1}	$Y = AB$
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	1	1	0	1	1	0
1	0	0	0	0	1	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	1	1
1	1	1	1	1	0	0	1

Step 3 : Draw the state diagram :

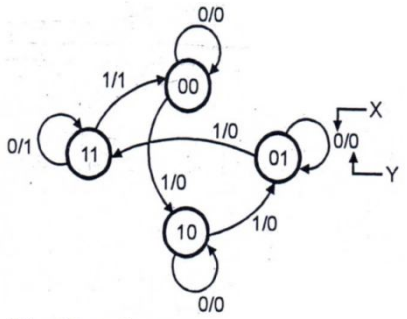


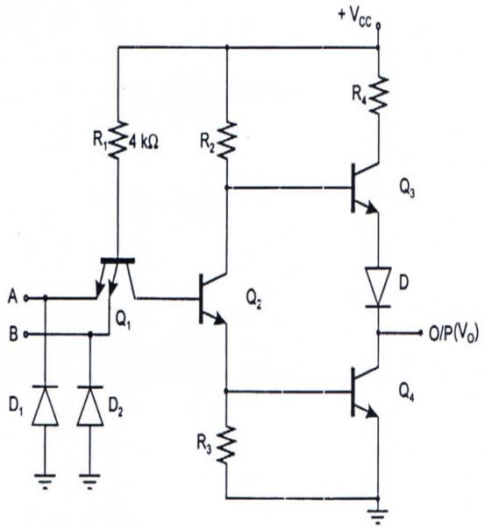
Fig. : State diagram

4. Attempt any ONE part of the following : (1*5 = 5)

a) Define the following terms. **(i)** Fan-out **(ii)** Propagation Delay. Draw the circuit of two input TTL NAND gate.

Answer : (i) Fan-out : The fan-out of a logic gate is defined as the maximum number of standard loads that the output of the gate can drive without impairing its normal operation.

(ii) Propagation Delay : A Pulse through a gate takes a certain amount of time to propagate from input to output. This interval of time is known as the Propagation Delay.



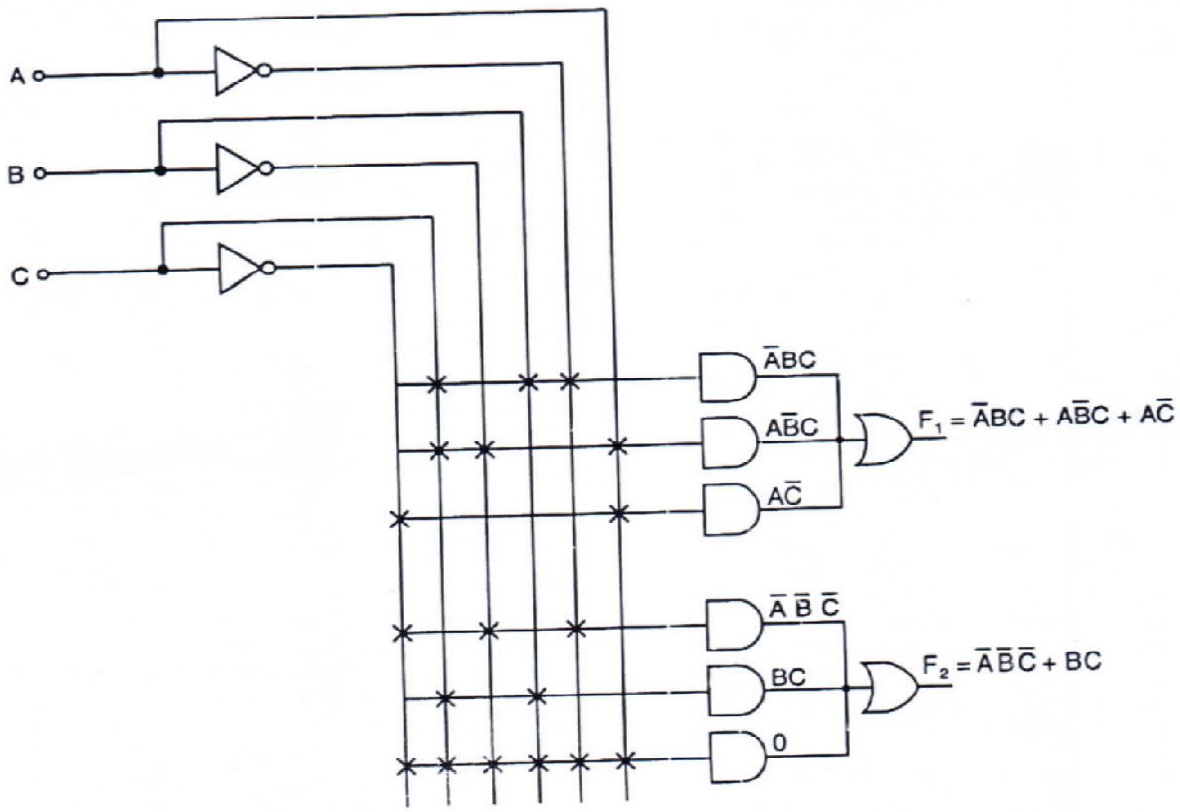
Two input TTL NAND Gate

b) Show how the PAL circuit is programmed to implement and function

$$F_1 = \bar{A}BC + A\bar{B}C + A\bar{C}$$

$$F_2 = \bar{A}\,\bar{B}\,\bar{C} + BC$$

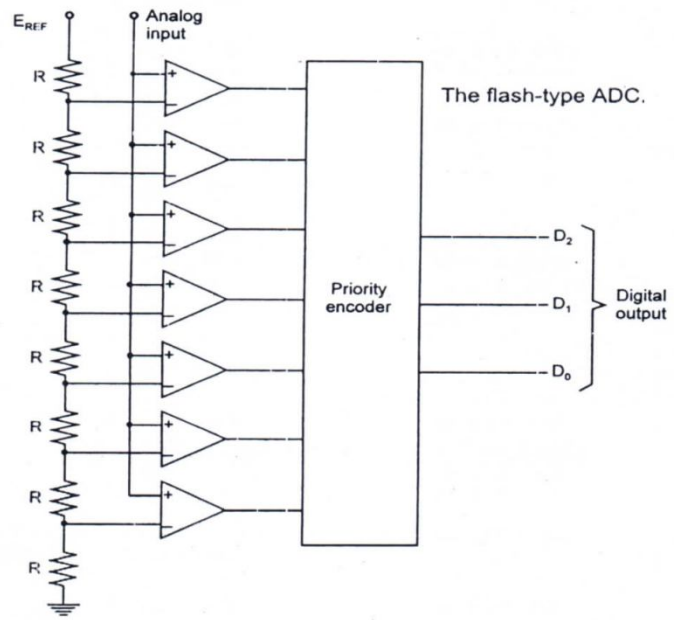
ANSWER :



5. Attempt any ONE part of the following : **(1*5 = 5)**

a) Draw and Explain the working of Flash-Type A/D converter.

ANSWER :



THE FLASH-TYPE A/D CONVERTER

The flash (or simultaneous or parallel) type A/D converter is the fastest type of A/D converter.

This type of converter utilizes the parallel differential comparators, that compare reference voltages with the analog input voltage.

an n-bit converter of this type requires $2^n - 1$ comparators,

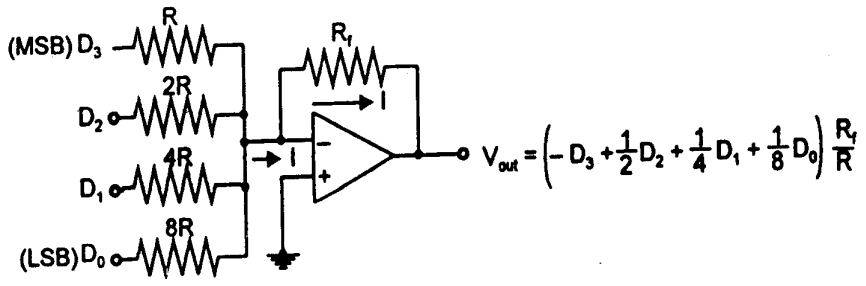
2^n resistors, and a priority encoder.

A reference

voltage E_{REF} is connected to a voltage divider that divides it into seven equal increment levels. Each level is compared to the analog input by a voltage comparator.

b) Draw and explain the schematic circuit of Weighted Resistor Type DAC.

Answer : The diagram is shown in fig.



Weighted Resistor Type DAC

The operational amplifier is used to produce a weighted sum of the digital inputs, where the weights are proportional to the weights of the bit position of inputs. Since the op-amp is connected as an inverting amplifier, each input is amplified by a factor equal to the ratio of the feedback resistance divided by the input resistance to which it is connected. The MSB D_3 is amplified by R_f/R, D_2 is amplified by $R_f/2R$, D_1 is amplified by $R_f/4R$, and D_0, the LSB is amplified by $R_f/8R$.

$$V_{out} = -\left(D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right) \times \left(\frac{R_f}{R}\right)$$